Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – WINTER • 2013

Subject code: 730204 **Date: 28-11-2013**

Subject Name: Embedded Systems

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Define Embedded System with Real Time Behavior & Current trends in Embedded Systems.	**07**
	(b)	What are the types of Real Time Systems and define the deadline for a hard Real Time System?	**07**
Q.2	**(a)**	How different tools take various input files and generate appropriate output files to ultimately be used in building an executable image?	**07**
	(b)	What are basic steps required to execute an image from RAM after transfer from ROM.	**07**
		OR	
	(b)	Discuss the role of RTOS in Interrupt Handling and Task Scheduling.	**07**
Q.3	**(a)**	With a neat diagram explain the advance RAM architecture. Also explain how this is extended to improve the performance through synchronous DRAM.	**07**
	(b)	Show and explain the interfacing of system buses between the processor, memory and I/O devices.	**07**
		OR	
Q.3	**(a)**	Explain Schedulability Analysis. Also implement the equation for three tasks T1, T2 and T3 with respective execution time 20, 30 and 50 and period (milliseconds) 100,150 and 300 respectively. Find the processor utilization.	**07**
	(b)	With a neat diagram explain the architecture of a general purpose processor.	**07**
Q.4	**(a)**	Sketch and define programmable interrupt controller and discuss how to handle exceptions and interrupts.	**07**
	(b)	Explain Fault tolerant system and also write the pseudo-code for Wait and Signal Operations.	**07**
		OR	
Q.4	**(a)**	Explain Synchronous and Enhanced Synchronous DRAM. Show how to use a 1K×8 ROM to implement a 512×6 ROM.	**07**
	(b)	Design a parallel I/O peripheral for the ISA bus. Provide : (i) A State Machine Description and (ii) A Structural Description	**07**
Q.5	**(a)**	Explain Hardware/Software Co-Simulation. What is the key method for speeding up such simulation?	**07**
	(b)	Explain Finite State Machine with example. Design the elevators unit control process using a state machine.	**07**
		OR	
Q.5	**(a)**	Show how using the process create and join semantics one can emulate the procedure call semantics of a sequential programming model.	**07**
	(b)	Explain the role of timers in Embedded System.	**07**

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