Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – WINTER • 2013

Subject code: 730303 **Date: 28-11-2013**

Subject Name: VLSI Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q-1	a)	Design 3 bit up counter using T flip-flop and write Verilog HDL code for 3 bit up counter.	10
	b)	Compare Verilog and VHDL	04
Q-2	a)	Write verilog HDL code for half adder using data flow structure and behaviour modelling.	06
	b)	List and explain any four Verilog relational operators	08
		OR	
	b)	Explain following key word with one example i) reg ii) integer iii)time iv) real	08
Q-3	a)	Design and explain the block diagram of addition of two 4 bit data with example.	07
	b)	Write verilog code for following sequences continuously repeat 10, 2, 5, 8, 12, 11,14, 3, 6, 7, 1, 13, 15	07
		OR	
Q-3	a)	Write Verilog HDL code for two 4 bit data using Verilog code of full adder.	07
	b)	Design and write Verilog HDL code for negative edge sensitive S-R flip-flop.	07
Q-4	a)	List and explain any four Unary Reduction Operators.	07
	b)	Define “function”. Explain it with one example	07
		OR	
Q-4	a)	Draw block diagram of 64 K ROM with verilog HDL code	07
	b)	Explain following instructions with one example. i) For ii) while iii) repeat	07
Q-5	a)	Compare following *i)* PLA & PLD ii) FPGA & CPLD	07
	b)	Write Verilog code for 8x3 encoder.	07
		OR	
Q-5	a)	Write Verilog code for 1x8 demultiplexer	08
	b)	Differentiate between logical and arithmetic ANDing, ORing and NOTing with one example	06

****