Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – WINTER • 2013

Subject code: 730406 **Date: 28-11-2013**

Subject Name: Peripheral System Design and Interfacing

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain GPIB bus configurations with their advantage and disadvantage.	**07**
	(b)	List various schemes for memory contention control of a CRT display system. Explain CRT display system with transparent addressing.	**07**
Q.2	**(a)**	Explain serial communication using null modem and loop back plug.	**07**
	(b)	Give the classification of GPIB bus signal. Explain each signal in brief.	**07**
		OR	
	(b)	Explain in detail different GPIB polling methods.	**07**
Q.3	**(a)**	Why address contention circuits are required in CRT controller? Explain MPU priority and Φ1 / Φ2 interleaving scheme.	**07**
	(b)	What do you mean by bus? Explain bus structure and bus design in detail.	**07**
		OR	
Q.3	**(a)**	Explain frame synchronism using RES signal in CRT controller.	**07**
	(b)	Explain in detail EISA, MCA, PCI and VESA VL bus.	**07**
Q.4	**(a)**	Write short notes on "programmable logic controllers"	**07**
	(b)	State different serial port's registers of PCs. Explain any three of them in detail.	**07**
		OR	
Q.4	**(a)**	What is data acquisition system? Draw and explain block diagram of it in detail.	**07**
	(b)	Explain in detail ECR with bit assignments w.r.to. parallel port	**07**
Q.5	**(a)**	Explain different program development tools used in µp based system with models.	**07**
	(b)	Draw functional block diagram of DMA controller & explain DMA operation.	**07**
		OR	
Q.5	**(a)**	Explain in detail different modes of parallel port in BIOS.	**07**
	(b)	Explain program development process in detail with flow chart used in µp based system.	**07**

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