Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – WINTER • 2013

Subject code: 732604 **Date: 28-11-2013**

Subject Name: Low –power CMOS VLSI Circuit Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is the need of Variable Threshold CMOS (VTCMOS) circuits? Discuss VTCMOS circuits in detail.	**07**
	(b)	Explain Current-Mode Adders.	**07**
Q.2	**(a)**	Discuss short- circuit dissipation in active power dissipation.	**07**
	(b)	Discuss standby leakage control using transistor stacks (self reverse bias)	**07**
		OR	
	(b)	Discuss Carry Select Adders (CSL) and compare its performance with Ripple Carry Adder (RCA).	**07**
Q.3	**(a)**	Discuss Baugh-Wooley multiplier with its basic building blocks.	**07**
	(b)	Discuss Electrically Erasable Programmable ROM (EEPROM) cell.	**07**
		OR	
Q.3	**(a)**	Discuss Reduction of Switched Capacitance in Low-power CMOS Logic circuits.	**07**
	(b)	Discuss Fowler-Nordheim tunneling.	**07**
Q.4	**(a)**	Discuss low power techniques at architecture level and circuit level for ROM.	**07**
	(b)	Draw and discuss conventional current sense amplifier	**07**
		OR	
Q.4	**(a)**	Discuss the operation of Shared-BL SRAM cell and explain the cause of increased access time.	**07**
	(b)	Discuss Booth's algorithm for multiplication.	**07**
Q.5	**(a)**	Discuss 16-bit Carry Skip Adders using 4-bit skip blocks.	**07**
	(b)	Discuss Precharge and equalization circuit in SRAM.	**07**
		OR	
Q.5	**(a)**	List the types of DRAM, and discuss any two in brief.	**07**
	(b)	Explain architecture–driven voltage scaling for low power designs	**07**

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