Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – WINTER • 2013

Subject code: 732902 **Date: 28-11-2013**

Subject Name: VLSI Circuits and Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** 1. Draw and explain different region for MOSFET C-V characteristics. **09**

2. What are the concepts of Locality, Design Hierarchy & Modularity?

3. Fill in Blanks.

(i) VLSI Design is _____

(a) A parallel process with no feedback loop

(b) A parallel process with feedback loop

(c) a sequential process with no feedback loop

(d) none of these

(ii) CAD tools _____ the VLSI design.

(a) Reduce design cycle time

(b) automate

(c) all of these

(d) none of these

(iii) According to Moore's law, the number of components doubles in every _____ months.

(a) ten

(b) twenty

(c) eight

(d) none of these

(b) Define minimum feature size. Enlist & explain the parameters to measure the design quality. **05**

Q.2 **(a)** Explain in detail voltage bootstrapping with neat sketches. **07**

(b) Define Latch-Up. What are the parameters that create Latch-Up.? How it is avoided. **07**

OR

(b) (1) Compare FPGA & CPLD for various aspects. **07**

(2) Compare FPGA & ASIC for various aspects.

Q.3 **(a)** Explain the concept of switching activity with neat diagram. **07**

(b) What do you mean by MOSFET modeling? Enlist MOSFET models. Explain any one in details. **07**

OR

Q.3 **(a)** Calculate the threshold voltage for a polysilicon gate nMOS transistor with the following parameters:- **07**

$N_A = 2 * 10^{16}$ cm^{-3} , $N_D = 2 * 10^{19}$ cm^{-3},

$N_{ox} = 2 * 10^{10}$ cm^{-2}, $t_{ox} = 300$ Å

(b) Write a detailed note on oxide related capacitances. **07**

Q.4 **(a)** What are the features of BiCMOS? Implement a two- input NOR logic using **07**

BiCMOS.

	(b)	Draw & explain BiCMOS architecture to implement any complex binary logic.	**07**

OR

Q.4	**(a)**	State advantages & disadvantages of BiCMOS. Also list out applications of BiCMOS.	**07**
	(b)	Explain the concept of observability & controllability? Write a testing sequence for Scan Based Techniques.	**07**
Q.5	**(a)**	Explain the design of (1) two-input NOR gate (2) two-input NAND gate	**07**
	(b)	Explain in details Current monitoring I_{DDQ} Test.	**07**

OR

Q.5	**(a)**	Design AND/NAND gate using CPL.	**07**
	(b)	Explain the following process for VLSI fabrication with sketches:- (i) Diffusion (ii) Etching (iii) Photolithography	**07**

****