Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – WINTER • 2014

Subject code: 1710412 **Date: 05-12-2014**

Subject Name: Digital VLSI Design

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain NAND Gate using CMOS, pass and CPL logic.	**07**
	(b)	Write short note on CMOS NOR2 Gate. Explain its usefulness.	**07**
Q.2	**(a)**	Explain typical fabrication process of MOSFET.	**07**
	(b)	Explain in short (i) Difference between AOI and OAI. (ii) Difference between Pass and CPL. (iii) Stick diagram layout of CMOS NOR2.	**07**
		OR	
	(b)	Compare energy band diagram for the components that make up the MOS transistor. Draw and explain energy band diagram of the combined MOS system.	**07**
Q.3	**(a)**	Draw resistive load nMOS inverter. Discuss its voltage transfer characteristic with important points. Comment on power and area consideration of resistive load nMOS inverter.	**07**
	(b)	Explain RC delay model for CMOS inverter with appropriate diagram and explain how rise time and fall time are computed if inverter is driving another inverter.	**07**
		OR	
Q.3	**(a)**	Write short note on Interconnect parasitic.	**07**
	(b)	Sketch $Y = \overline{(A \cdot B + C) \cdot D}$ with transistor widths chosen to achieve effective rise and fall resistance equal; to a unit inverter. Also sketch RC delay model for same.	**07**
Q.4	**(a)**	Explain VLSI design flow and hierarchy.	**07**
	(b)	Explain dynamic NOR gate with diagram.	**07**
		OR	
Q.4	**(a)**	Explain in short (i) Inversion (ii) Depletion Depth. (iii) Channel Length Modulation.	**07**
	(b)	Explain behavior of bistable elements.	**07**
Q.5	**(a)**	Explain D Flipflop with appropriate diagram and waveforms. Draw MOS transistor level schematic.	**07**
	(b)	Stick diagram layout of CMOS NAND2.	**07**
		OR	
Q.5	**(a)**	Describe resistive load inverter circuit with layout.	**07**
	(b)	Explain 2 input CMOS full adder circuit with layout.	**07**

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