Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE / ME / MBA / MCA - SEMESTER– • EXAMINATION – WINTER 2014

Subject Code:2710507 **Date:12/01/2015**

Subject Name: ASIC Design

Time: **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

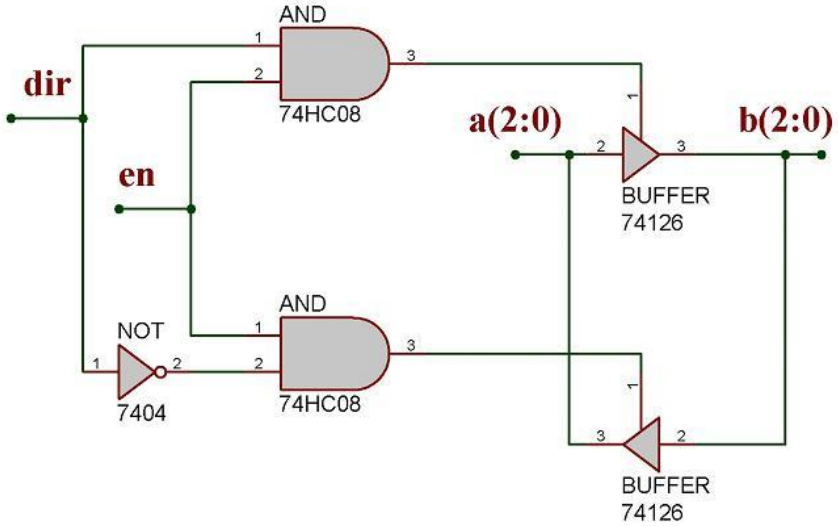
Q.1		Do as directed. (Two marks each)	**14**
	1	Derive subtypes from std_logic_vector to represent a nibble and byte. Define nibble objects N and byte object B. Transfer contents of N to the upper nibble of B in reverse order.	
	2	Consider the following declaration. signal A: std_logic_vector(3 downto 0) := "1011"; signal B : std_logic_vector(0 to 3) := "1011"; What will be the value of B(3), B(1), A(3) and A(0)?	

	3	Consider the following declaration.
		type mem is array(3 downto 0) of std_logic_vector(7 downto 0);
		constant ROM: mem := ("10101010", "10101111", "10100000", "11001100");
		signal data: std_logic_vector(7 downto 0);
		data <= ROM(2);
		What will be the value of data after execution of above statement?	

	4	State importance of wait statement in VHDL.	
	5	What do you mean by generic mapping and what is the use of it?	
	6	Write entity declaration of 1x4 demultiplexer.	
	7	What is use of package in VHDL?	
Q.2	**(a)**	Explain (i) Full Custom ASIC (ii) Standard cell based ASIC (iii) Gate-Array based ASIC with appropriate diagram.	**07**
	(b)	With diagram compare and explain ROM, PLA and PAL programmable logic devices.	**07**
		OR	
	(b)	Compare CPLD and FPGA with appropriate diagram.	**07**
Q.3	**(a)**	Write VHDL code for D-latch with behavioral modeling. Use D-latch as component and implement 4-bit register using same. Use generate statement.	**07**
	(b)	Write VHDL code for parallel to serial converter. Data is of 8 bit. Serial output consist start bit, 8 data bits, parity bit and stop bit.	**07**
		OR	
Q.3	**(a)**	Write VHDL code to implement 16-bit universal shift register, which supports shift-left, shift right, and parallel-in modes.	**07**
	(b)	Write VHDL code of 2x4 decoder using following constructs. (i) when é . Else (ii) case é . when.	**07**

Q.4 **(a)** Consider finite state machine with one input X and one output Z. The FSM asserts its output Z when it recognizes the following input bit sequence: "1011". The machine will keep checking for the proper bit sequence and does not reset to the initial state after it has recognized the string. As an example the input string X= "..1011011..." will cause the output to go high twice: Z = "..0001001.." . Draw State diagram, state table and write VHDL code. **07**

(b) Write behavioral VHDL code for the circuit shown in figure below. **07**



OR

Q.4 **(a)** Draw the block schematic of the circuit implemented by the following VHDL code in terms of known combinational and sequential blocks. **07**

```
library ieee;
use ieee.std_logic_1164.all;
        entity abc is port
        clk,rst,din: in std_logic;
        X,Y: out std_logic);
        End abc
architecture exam of abc is
Signal s1,s2,s3,s4,s5: std_logic;
begin
  process (clk,rst)
  begin
        if (rst=ô1ô) then s2 <= (others => ó0ô);
        Else if (clk ôevent and clk = ô1ô) then
                s2<=s1;
                s3<=s2;
                s5<=s4;
        End if;
 s1 <= din xor s5;
 s4 <= s3 xor s5;
end process;
   X<=s2;
   Y<=s3;
End exam
```

(b) Draw state diagram and write VHDL code for ñ10ò sequence detector using both moore and mealy FSM. **07**

Q.5	**(a)**	Write short note on Various Loops in VHDL.	**07**
	(b)	Explain delta delay, inertial delay and transport delay. State their importance in digital circuit design.	**07**

OR

Q.5	**(a)**	What are the advantages of using a hard ware description language? State important features of VHDL.	**06**
	(b)	Differentiate signal and variable in VHDL with appropriate example.	**04**
	(c)	For given below VHDL code show waveforms for signal a, x, y and z	**04**

```
entity delaym is
end entity;
architecture arch_delaym of delaym is
signal a, x, y, z: bit;
begin
        a <=    ó1ô after 5ns, ó0ô after 10 ns,
                        ó1ô after 18 ns, ó0ô after 22 ns,
                        ó1ô after 28 ns, ó0ô after 30 ns,
                        ó1ô after 32 ns, ó0ô after 38 ns;
x <= a after 5 ns;
y <= reject 3 ns inertial a after 5 ns;
z <= transport a after 5 ns;
end arch_delaym;
```

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