Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY M. E. - SEMESTER – I • EXAMINATION – WINTER • 2014

Subject code: 2712605 Subject Name: Physics of MOS Transistor Time: 02:30 pm - 05:00 pm

Total Marks: 70

Date: 09-01-2015

Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.
- Q.1
- (a) Characteristics for n-channel MOSFET on a log and linear I_D axis for various values of V_{GS}. Clearly indicate all three regions in your plot; 1. Strong inversion, 2. Moderate inversion and 3. Weak inversion.
 (b) Explain/define followings terms: 1. Degenerate semiconductors, 2. 03 Transit time, and 3. Velocity saturation.
 - (b) Define various capacitances in MOS capacitor system and obtain exact 07 expressions for C ϕ and C ϕ .
- Q.2 (a) Draw the structure of p-type substrate MOS capacitor and explain the effect 07 of change in V_{GB} on surface potential. Derive expression for electron concentration at the surface as a function of surface potential.
 - (b) 1. Sketch three-terminal MOS structure (p-type substrate) and its energy 04 band diagram for the following: 1. $V_{CB} = 0$ and 2. $V_{CB} > 0$. Assume $V_{GB} > V_T$. 03 2. Sketch surface potential versus V_{-} for three terminal MOS structure for

2. Sketch surface potential versus V_{CB} for three-terminal MOS structure for a particular value of V_{GB} . Indicate V_Q , V_W , and V_U in the diagram.

OR

- (b) Obtain simplified general expressions for inversion and depletion charges for p-type substrate MOS capacitor system operating in inversion region and plot them as a function of surface potential. Assume that the device is not operating in accumulation region.
- Q.3 (a) Define body effect parameter in three-terminal MOS structure. Explain 07 qualitatively the effect of increase in V_{CB} on inversion layer charge and why for a given increase in V_{CB} , V_{GC} is to be increased by a larger value compared to an increase in V_{CB} for higher doping and thicker oxide to maintain the same inversion layer charge.
 - (b) Derive accurate strong inversion model (basis of level 2 model in Berkeley 07 Spice Simulator) for four-terminal p-type substrate MOS structure.

OR

- Q.3 (a) Obtain expression of inversion charge for three-terminal p-type MOS 07 structure operating weak inversion region.
 - (b) Discuss the effect of parameter on the accuracy of simplified strong 07 inversion model.
- Q.4 (a) Discuss the effects of temperature change on \div ONøcurrent, leakage current, 07 and V_T of MOSFET device with necessary diagrams.
 - (b) What do you understand by hot carrier effect? How does it affect drain and 07 bulk current? Draw a plot of I_{DB} as a function of V_{GS} at different values of V_{DS} . How can we reduce hot carrier effect?

- Q.4 (a) Derive Level 3 MOSFET model for the drain current flowing through 07 MOSFET device. Write down level 1 equation for the drain current from level 3.
 - (b) Show that due to velocity saturation effect, the drain current in shortchannel MOSFET does not follow square-law. Also justify that the ratio of (W/L) of PMOS and NMOS devices is less than 2 for equal driving capability in short-channel devices.
- Q.5 (a) Discuss different components of source/drain resistance and derive 07 expression for I_{DS} taking into account effects of source/drain resistance.
 - (b) Explain MOSFET parameter extraction. How would you extract $V_{T}, \ _{0}, \ 07$ $V_{FB}, \mbox{ and } .$

OR

- Q.5 (a) Define drain-induced barrier lowering (DIBL). Derive the expression for the 07 drop in threshold voltage in short-channel MOSFET device compared to long-channel device for deep source/drain regions due to DIBL.
 - (b) The gate of MOSFET is applied with pulse signal having finite rise and fall 07 time. Assume that the rise time is greater than the fall time. Also assume that the frequency of input signal is very low and MOSFET operates in quasi-static region. Plot drain and source currents as a function time. Make important comments.
