Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER • 2014

Subject code: 2715410 **Date: 12-01-2015**

Subject Name: Advanced Digital Circuit Design

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Briefly discuss Digital Circuit Implementation Approaches. Also compare Full custom and Semi-custom mask layout.	**07**
	(b)	List the different abstraction level of digital design. Also give difference between Top- Down and Bottom- Up methodologies for digital system.	**07**
Q.2	**(a)**	Draw and explain operation of the 2-input NOR Gate using CMOS Topology and Derive the necessary equationôs for the same.	**07**
	(b)	Briefly discuss the different ways of the timing control in Verilog.	**07**
		OR	
	(b)	What do you understand by gate Delays. Also define and compare Rise Delay and Fall Delay with suitable examples and waveforms**.**	**07**
Q.3	**(a)**	Draw the Gate level schematic and CMOS Implementation of D-latch and clocked JK latch also draw the truth table for its operation modes of transistors.	**07**
	(b)	Explain blocking and non-blocking statement with suitable example and also give the points of difference between task and function.	**07**
		OR	
Q.3	**(a)**	Discuss data types used in Verilog in brief.	**07**
	(b)	Write the Verilog code to implement ALU with given specifications. (There are two data each of 4 bits and two bits control line and If control is ó00ô must do addition,ô01ô substraction,ô10ô multiplication,ô11ô division)	**07**
Q.4	**(a)**	Write a Verilog code for 8-Bit Parallel in Serial out and serial in parallel out Shift Register.	**07**
	(b)	Give the difference between Moore and Mealy machine also write the Verilog code for serial parity detector using Moore machine.	**07**
		OR	
Q.4	**(a)**	What is scheduling? Also briefly discuss about various scheduling algorithms.	**07**
	(b)	Explain multilevel logic minimization approaches with examples.	**07**
Q.5	**(a)**	What do you understand by technology mapping? Explain Programmable Logic devices. Also Give Comparison between various technologies.	**07**
	(b)	Explain behavioral Modeling of Verilog. Also Write Verilog code for Master-slave JK flips flop.	**07**
		OR	
Q.5	**(a)**	What is the need for floor planning and Placement tools? Discuss the core objectives and goals of Floor Planning.	**07**
	(b)	Discuss techniques for partitioning and routing in brief.	**07**

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