Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– I• EXAMINATION – WINTER 2014

Subject Code: 3715201 **Date:06/01/ 2015**

Subject Name: Advanced Computer Architecture

Time: 2:30 to 5:00 Pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Write a short note on Classes of Computers	**07**
	(b)	Explain 3 stage pipeline in ARM architecture	**07**
Q.2	**(a)**	Explain Control Dependences in detail.	**07**
	(b)	Explain the below mentioned concepts and differentiate them. 1.RISC and CISC 2. Big-endian and Little-endian.	**07**
		OR	
	(b)	Writ e about caches memory? Why Caches memory is required?	**07**
Q.3	**(a)**	List advantages & disadvantages of On chip RAM	**07**
	(b)	What is Snoop control unit (SCU).	**07**
Q.3	**(a)**	Draw block diagram of Unified instruction and data cache	**07**
	(b)	Explain about Translation Look-Aside Buffer	**07**
Q.4	**(a)**	Explain for Bus architecture with the Architecture Diagram	**07**
	(b)	Draw block diagram of Harvard architecture based data an instruction caches	**07**
		OR	
Q.4	**(a)**	Write about Memory Organization in System architecture?	**07**
	(b)	Explain different Multi-processor architecture?	**07**
Q.5	**(a)**	Give the difference between INTEL,ARM, Power PC architecture	**07**
	(b)	Explain about the SPARC and Power PC architectures	**07**
		OR	
Q.5	**(a)**	Explain about Basic VLIW Design Principles? What are Implications for Compilers design in VLIW.	**07**
	(b)	What is a tool chain? What are essential components of a tool chain and explain each.	**07**

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