Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – WINTER • 2014

Subject code: 3715204 Date: 12-01-2015

Subject Name: Digital VLSI Design and Verification - I

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Design a state machine to detect the sequence 11011 with overlapping and non-overlapping sequence. **07**

(b) For the below line of codes, what will be the synthesized output and justify your answer? **07**

Consider in1 as input, out1 as output and reg1 as register.

a) always@(posedge clock) clock)

```
begin
    reg1<=in1;
    out1<=reg1;
end
```

b) always@(posedge clock) clock)

```
begin
    reg1<=in1;
    out1=reg1;
end
```

c) always@(posedge

```
begin
    reg1 =in1;
    out1<=reg1;
end
```

d) always@(posedg

```
begin
    reg1 =in1;
    out=reg1;
end
```

Q.2 **(a)** What is metastability? What are the different cases metastability occur? How to avoid it? **07**

(b) What do you understand by noise margin? Draw the voltage transfer characteristic of an inverter and clearly show VIH, VIL, VOH, and VOL and write the equation for NM_H and NM_L. **07**

OR

(b) Draw the layout for the below Boolean equations. **07**

a) Y=~(a+bc) b) Y=~(ab+cd)

Q.3 **(a)** What is synthesis? Explain the different inputs we need to consider while doing synthesis and also explain the outputs generated by the synthesis tool. **07**

(b) Explain the FPGA design flow and mention the tools used by XILINX for each step. **07**

OR

Q.3 **(a)** Explain the different steps involved in physical design flow? **07**

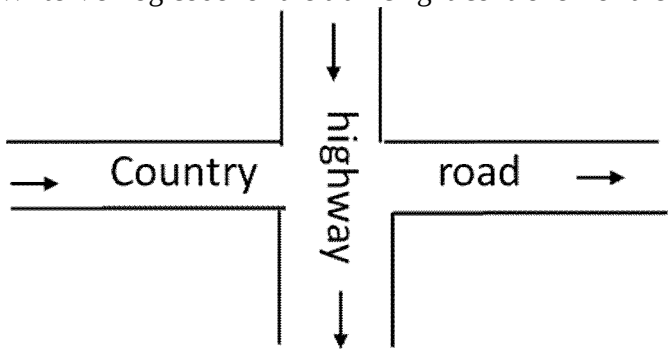
(b) What is static timing analysis? Explain the difference between STA and DTA? **07**

Q.4 **(a)** Explain the design of FIFO with the help of block diagram, assume that you are using FIFO in between two clock domains of different frequency. **07**

(b) What is an IP? Explain different types of IP? Explain the need of IP in SOC by taking an example. **07**

OR

Q.4 **(a)** Write Verilog code for the traffic light controller for the below diagram. **07**



The folowing specification must be considered.
The traffic signal for the main highway gets highest priority. Thus, the main highway signal remains green by default.
Occasionally, cars from the country road arrive at the traffic signal. The traffic signal for the country road must turn green only long enough to let cars on the country road go.
As soon as there are no cars on the country road, the country road traffic signal turns yellow and then red and traffic signal on the main highway turns green again.
Assume there is a sensor to detect cars waiting on the country road. The sensor sends a signal X as input to the controller. X=1 if there are cars on the country road, otherwise ,X=0;

(b) Explain transport delay, inertial delay and delta delay in VHDL with example. **07**

Q.5 **(a)** Write short note on assertion based verification. In what way, this method is supported by Verilog, VHDL and System Verilog. **07**

(b) Write short note on **07**
a) NRE cost and recurring cost. b) Yield and technology scaling.

OR

Q.5 **(a)** Write short note on **07**
a)Full custom design b)standard cell based and gate array based design

(b) Explain the difference between verification and testing? Explain different levels of testing? And also explain test generation and fault models. **07**