GUJARAT TECHNOLOGICAL UNIVERSITY M. E. - SEMESTER – I • EXAMINATION – WINTER • 2014

| Subject code: 3/15501 Date: 06-01-2 | | | |
|-------------------------------------|------------|---|----------|
| Ti | • | Name: Advanced Computer Architecture 2:30 pm - 05:00 pm Total Marks: 70 | |
| ms | | Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks. | |
| Q.1 | (a) (b) | What are the CPU ó GPU Synchronization issues Explain 3 stage pipeline in ARM architecture | 07 07 |
| Q.2 | (a) (b) | Explain Data Hazard in detail. Explain the below mentioned concepts and differentiate them. 1.RISC and CISC 2. Big-endian and Little-endian. OR | 07 07 |
| | (b) | Explain cache coherency in detail? | 07 |
| Q.3 | (a) (b) | Describe in brief Interrupt Controller MPCore processors Explain SIMD instructions in brief OR | 07 07 |
| Q.3 | (a) (b) | Draw block diagram of Unified instruction and data cache What is Snoop control unit (SCU). | 07 07 |
| Q.4 | (a) | Draw block diagram of Harvard architecture based data and instruction caches | 07 |
| | (b) | List down 3 major Bus Transactions and explain OR | 07 |
| Q.4 | (a) (b) | Explain about Translation Look-Aside Buffer Describe a typical TLB Format | 07 07 |
| Q.5 | (a) (b) | Explain memory Segmentation (related to MMU) in brief Explain Paging memory management ?How Paging related to MMU OR | 07 07 |
| Q.5 | (a) | Explain about Basic VLIW Design Principles? What are Implications for Compilers design in VLIW. | 07 |
| | (b) | What is a toolchain. What are essential components of a toolchain and explain each. | 07 |
