GUJARAT TECHNOLOGICAL UNIVERSITY M. E. - SEMESTER – I • EXAMINATION – WINTER • 2014

	Sub	oject code: 714103N Date: 03-12-2014 oject Name: Digital Signal Processor Architecture ne: 10:30 am - 01:00 pm Total Marks: 70	
		 ructions: 1. Attempt all questions. 2. Make suitable assumptions wherever necessary. 3. Figures to the right indicate full marks. 	
Q.1.	(a)	Define the following terms with example with reference to discrete time systems:	[7]
	(b)	(i)Causality (ii) Stability (iii) Linearity Write the main advantages of digital signal processing.	[7]
Q.2.	(a) (b)	Explain the decimation in time algorithm for 8 point FFT. Compare overlap add and overlap save methods. OR	[7] [7]
	(b)	Explain the finite word length effect in digital filters.	[7]
Q.3.	(a) (b)	Explain Von Neumann architecture and Harvard architecture with block diagram. Explain Very Long Instruction Word architecture with proper block diagram. OR	[7] [7]
Q.3.	(a)	Write at least five addressing modes used in programmable DSPs and explain any two of them.	[7]
	(b)	Explain the following on-chip peripherals with reference to programmable DSPs: (i)TDM serial port (ii) Host Port (iii) ADC	[7]
Q.4.	(a) (b)	Draw only the internal bus architecture of TMS320C5X. Explain the Central Arithmetic Logic Unit and Auxiliary Register ALU of TMS320C5X. OR	[7] [7]
Q.4.	(a)	Give the brief description of the following 5X instructions:	[7]
	(b)	LACB, LDP, PAC, BLDP, MPY, ANDB, ROL Write an assembly program to convolve the two sequences x(n), y(m) of length N=5 and M=3 respectively. x(n)=1, 2, 3, 2, 1 and y(m)=3, 4, 5	[7]
Q.5.	(a) (b)	Write the main features of TMS320C6X processors. Draw only the internal architecture of TMS320C6X processor. OR	[7] [7]
Q.5.	(a) (b)	Write the short note on Multi channel buffered serial port. Explain any one application with detail where DSP processor is utilized.	[7] [7]
