Seat No.: _____ Enrollment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. – SEMESTER – III • EXAMINATION-– WINTER • 2014

Subject code: 730303 **Date: 27-11-2014**

Subject Name: VLSI Design (Major Elective – IV)

Time: 02:30 pm – 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary and mention it clearly.**
3. **Appropriate comment lines are must in your program.**
4. **Figures to the right indicate full marks.**

Q.1		Design sequence detector to detect a bit sequence of ñ10101ò using Mealy Finite state Machine (FSM). Draw state diagram and write verilog code of the same.	**14**
Q.2	**(a)**	Write verilog code of positive edge triggered J-K flip-flop having asynchronous reset.	**07**
	(b)	Write verilog code of 8 inputs multiplexer having enable (EN) input using dataflow modeling style. When EN is high, output should be in high impedance state.	**07**
		OR	
	(b)	Write verilog code of 4 input multiplexer using conditional operator.	**07**
Q.3		Design modulo 13 counter using T - flip-flop with the help of flip-flop excitation table. Draw circuit diagram and write verilog code of the same using structural modeling style. Write verilog module of all components used in the design.	**14**
		OR	
Q.3		The traffic signals have two lights red and green. The major road (heavy traffic) normally has a green light while the minor road has a red light. If a car is detected on the minor road, the signal changes to red for the major and green for the minor road. When the lights change, a timer is started and when the timer completes, a ñtimedò signal is asserted which causes the light to change back to their default states. Draw state machine diagram and write verilog code of the same.	**14**
Q.4	**(a)**	Explain sequential blocks and parallel blocks with the help of appropriate example of each.	**07**
	(b)	Write verilog code of a negative edge triggered D-flip-flop having synchronous clear as active high signal. Use behavior statements only.	**07**
		OR	
Q.4	**(a)**	Explain three different ways of specifying delays in continuous assignment statements with the help of appropriate example of each,	**07**
	(b)	Write verilog code of BCD to seven segment decoder. If input is non BCD then display 'E' on seven segment.	**07**
Q.5	**(a)**	Explain in detail the architecture of Xilinx FPGA device with neat diagram.	**07**
	(b)	Write verilog code of the 8-bit universal shift register.	**07**
		OR	
Q.5	**(a)**	Write a function which calculates the odd parity of 16-bit address and returns a 1-bit value.	**07**
	(b)	Write verilog UDP description of positive edge triggered T-Flip-flop with active high asynchronous reset.	**07**

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