Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – WINTER • 2014

Subject code: 734202 Date: 27-11-2014

Subject Name: IC Fabrication Technology

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is Clean Room and why it is required? Write down the clean room classification as per federal standard 209 D.	**07**
	(b)	Explain the significance of alignment in photolithography and in detail explain the alignment techniques for mask layer.	**07**
Q.2	**(a)**	Explain the RCA wafer cleaning techniques. What is the effect of sodium as a surface impurity on NMOS transistor?	**07**
	(b)	Calculate the thickness X_{ox} of a layer SiO_2 grown on a bar <111> silicon wafer using steam at 100^{o} C for 1 hour for wet oxidation cycle. ($K=8.62 \times 10^{-5}$).	**07**
		OR	
	(b)	Calculate the thickness X_{ox} of a layer SiO_2 grown on a bar <100> silicon wafer using steam at 100^{o} C for 1 hour for wet oxidation cycle. ($K=8.62 \times 10^{-5}$).	**07**
Q.3	**(a)**	Explain the following terms with respect to wafer manufacturing. i. Ingot Shaping and Testing. ii. Crystal Metal Interface.	**07**
	(b)	What is PMMA? Explain the electron-beam Lithography.	**07**
		OR	
Q.3	**(a)**	Explain the following terms with respect to wafer manufacturing. i. Stress Release etching. ii. Back Side Treatment.	**07**
	(b)	What is Diffusion? Explain following techniques of diffusion. i. Pre-Deposition. ii. Drive-in.	**07**
Q.4	**(a)**	Explain the transport limited and reaction rate limited oxidation techniques and give the difference between them.	**07**
	(b)	What is sputtering? Explain DC magnetron sputtering to deposit AlSi films for shallow junction devices.	**07**
		OR	
Q.4	**(a)**	List down the different size of wafer and how we can identify it. What are the major obstacles to move from 300mm to 450mm size wafer?	**07**
Q.4	**(b)**	Explain why shallow junction is needed in smaller geometry devices for VLSI?	**07**
Q.5	**(a)**	Explain Plasma etching. Why anisotropic etching is required in VLSI.	**07**
	(b)	What is hot wall and cold wall CVD techniques? Which will be useful to deposit Si_3N_4, Ti and Ta on silicon?	**07**
		OR	
Q.5	**(a)**	Discuss CVD and PVD techniques to deposit metals and dielectric in the fabrication of high density VLSI circuit.	**07**
	(b)	How RC time constant is described in multilevel metallization scheme? Explain the effect of Low K dielectric on RC time constant.	**07**

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