Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC- SEMESTER–II - EXAMINATION – SUMMER 2017

Subject Code: X21102 **Date:01/06/2017**

Subject Name: DIGITAL LOGIC DESIGN DESIGN

Time: 10:30 AM to 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt any five questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the followings: **07**

1) Convert the number $(0.625)_{10}$ in to binary.
2) Convert $(A29)_{16}$ in to decimal.
3) Define positive logic.
4) Define negative logic.
5) If a 500 Hz square wave drives pin 3 of a 7404, what is the wave form of pin 4.
6) If a Low level is applied at pin 1 of 7408, what is the voltage at pin 3.
7) Write a truth table for Ex or gate.

(b) Define the following terms: Chip, Quad, Fan-out, Propagation delay, Literal, Nibble, Max term. **07**

Q.2 **(a)** Do as directed:

1) Justify "NAND gate as a universal gate". **03**
2) Using 10's complement subtracts: 72532 -3250. **02**
3) Using 9's complement subtracts: 72532-3250. **02**

(b) Express the Boolean function F = A + B'C in the sum of min-terms. **07**

Q.3 **(a)** List the disadvantage of K Map techniques. Reduce the following expression given Boolean function, F (A,B,C,D,E) = Σ(0,2,5,7,13,15,18,20,21,23,28,29,31) **07**

(b) Determine the prime-implicants of the given boolean function F(w,x,y,z) = Σ(1,4,6,7,8,9,10,11,15). **07**

Q.4 **(a)** What do you mean by combination logic circuit? Enlist the design steps. Obtain the logic circuit of the full substractor. **07**

(b) Write the significance of code conversion. Derive the BCD to excess-3 code converter. **07**

Q.5 **(a)** What do you mean by multiplexer? Implement F(A,B,C,D)= Σ(0,1,3,4,8,9,15) using multiplexer. **07**

(b) Write a brief note on PLA. **07**

Q.6 **(a)** What is race around condition? Explain the Master slave JK Flip flop. **07**

(b) Design a counter that has a repeated sequence of six state: 0,1,2,4,5,6 and repeat using JK Flip Flop. **07**

Q.7 **(a)** Write brief note on "Status Register" and draw the block diagram of an 8-bit ALU with a 4-bit status register. **07**

(b) Design a serial adder using a sequential logic procedure. **07**

****