Total Marks: 70

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC- SEMESTER-III - EXAMINATION – SUMMER 2017 Code: X31101 Date:25/05/2017

Subject Code: X31101

Subject Name: Advance Electronics

Time: 02:30 PM to 05:30 PM

Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.

Q.1	(a)	Draw and explain hybrid π model for CE configuration. Also explain validity of hybrid π model.	07
	(b)	Explain Emitter follower at higher frequency.	07
Q.2	(a) (b)	Explain classifications of amplifiers. Draw and explain RC coupled amplifier. Also draw frequency response of it. OR	07 07
	(b)	For CE short circuit current gain g_m = 50 mA/V, $r_{b'e}$ = 1 K Ω , C_e = 1 pF and C_c = 0.2 pF, determine the values of f_β and f_T .	07
Q.3	(a)	Three cascaded stage have an overall upper 3 dB frequency of 16 KHz and lower 3 dB frequency of 25 Hz. What are value of F_L and F_H of each stage? Assume that all the stages are identical. Also calculate bandwidth of each stage.	07
	(b)	Draw and explain block diagram of op-amp. OR	07
Q.3	(a)	In a transistorized Hartley oscillator the two inductors are 2 mH and 20 μ H while the frequency is to be changed from 950 KHz to 2050 KHz. Calculate the range over which the capacitor is to be varied.	07
	(b)	Draw and explain emitter-coupled differential amplifier.	07
Q.4	(a)	Draw circuit diagram of successive approximation ADC. Also explain working of it.	07
	(b)	Draw dual slop ADC. Also explain working of it. OR	07
Q.4	(a) (b)	Explain comparison of different logic families. Explain voltage series feedback with suitable example.	07 07
Q.5	(a)	 Define following terms. 1) Stability 2) Phase Margin 3) Feedback 4) Temperature drift 5) Input offset voltage 6) CMRR 7) Slew rate 	07
	(b)	Define Oscillator. Draw and explain Wien bridge oscillator circuit diagram. OR	07
Q.5	(a) (b)	List different characteristics of DAC and define it. Explain weighted resister type DAC.	07 07
