Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER– VI • EXAMINATION – SUMMER-2017

Subject Code: X61102 **Date: 02/05/2017**

Subject Name: VLSI Technology and Design

Time: 10.30AM to 01:00PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw and explain Y chart fort VLSI Design flow. Also draw simplified VLSI design flow at different abstraction levels.	**07**
	(b)	List and explain importance of different CAD tolls used for VLSI design.	**07**
Q.2	**(a)**	Explain n-well CMOS fabrication with necessary diagrams.	**07**
	(b)	Define design rules for layout design in VLSI Technology. List and explain types of design rules. Draw layout of CMOS inverter with necessary information.	**07**
		OR	
	(b)	Explain latch-up and its prevention in CMOS technology.	**07**
Q.3	**(a)**	Derive drain current equation in linear region and saturation region for NMOS.	**07**
	(b)	Define scaling in VLSI Technology.	**07**
		OR	
Q.3	**(a)**	Explain on chip clock generation and distribution.	**07**
	(b)	Explain difference between FPGA and CPLD.	**07**
Q.4	**(a)**	A CMOS inverter has $V_{TO,n}$ = 0.8 V, $V_{TO,p}$ = - 0.8 V , and k_n=k_p. Obtain $V_{IL,}$ V_{IH}, V_{OH},V_{OL} , NM_H and NM_L for V_{DD} = 5v .	**07**
	(b)	A CMOS inverter has $\mu_n c_{ox}$ = 120 µA/ V^2 $\mu_p c_{ox}$ = 60 µA/ V^2 , $V_{TO,n}$ = 0.8 V, $V_{TO,p}$ = - 1.0 V, T_{PHL} = 0.2 ns , T_{PLH} = 0.15 ns , V_{DD} = 3v C_{load} = 300 ff Determine (W/L)n and (W/L)p	**07**
		OR	
Q.4	**(a)**	Draw CMOS implementation for following Boolean equation $Z = \overline{A(D+E)+BC}$ Assume that (W/L)n = 10 for all NMOS and (W/L)p =15 for all PMOS. Find (W/L) equation for NMOS and PMOS.	**07**
	(b)	Draw and explain SR flip flop using CMOS Technology.	**07**
Q.5	**(a)**	Write short notes on built in self test techniques.	**07**
	(b)	Explain Basic Principles of pass transistor circuits.	**07**
		OR	
Q.5	**(a)**	Explain CMOS Dynamic Circuit Techniques.	**07**
	(b)	Write short notes on Adhoc Testable design techniques.	**07**

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