Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–II • EXAMINATION – SUMMER 2013

Subject Code: X21102 **Date: 10-06-2013**

Subject Name: Digital Logic Design

Time: 02.30 pm - 05.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4.

Q.1 **(a)** Do as directed: **07**

1. $(3FD)_{16}=(\quad)_8$
2. $(225.225)_{10} = (\quad)_2$
3. $(83)_9=(\quad)_5$
4. $(614)_7 = (\quad)_{10}$
5. $(11010111.110)_2 = (\quad)_{16}$
6. Obtain the 9's complement of $(864)_{10}$.
7. Find dual of x+1=1.

(b)

1. Add and multiply the $(135.4)_6$ and $(43.2)_6$ in the given base without converting to decimal. **03**
2. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction X-Y using 2's complements. **02**
3. Simplify the Boolean function F(x,y,z)=xy+xyz+xyz'+x'yz to a minimum number of literals by manipulation of Boolean algebra. **02**

Q.2 **(a)** Answer the following questions: **07**

1. Simplify the following Boolean function using Karnaugh map (in sum of products form):
   F(A,B,C,D)=A'B'D'+A'CD+A'BC and don't care conditions
   d=A'BC'D+ACD+AB'D'
2. Implement a full-adder circuit with a decoder and two OR gates.

(b) Simplify the Boolean function F(w,x,y,z)=Σ(0,1,2,8,10,11,14,15) using tabulation method. **07**

OR

(b) Design a combinational circuit that accepts a three-bit number and generates an output binary number equal to the square of the input number. **07**

Q.3 **(a)** Write brief note on full-subtractor and construct it using only NAND gates. **07**

(b) Write brief note on "Binary parallel adder". Also describe 4-bit full adder with look-ahead carry in detail. **07**

OR

Q.3 **(a)** Answer the following questions: **07**

1. Implement Boolean function F(A,B,C,D)=Σm(2,4,5,7,10,14) using 8:1 multiplexer.

2. Draw a combinational logic circuit, which can compare two 4-bit binary numbers.

(b) Explain operation of an edge triggered D flip-flop. **07**

Q.4 **(a)** Design a counter with the following binary sequence: 0, 1, 3, 2, 6, 4, 5, 7 and repeat. Use RS flip-flops. **07**

(b) What is meant by race-around condition in relation to the J-K flip-flops? Draw clocked Master-Slave J-K flip-flop configuration and explain it in brief. **07**

OR

Q.4 **(a)** Explain 4-bit bidirectional shift register with parallel load in detail. **07**

(b) Explain 4-bit synchronous up-down binary counter in detail. **07**

Q.5 **(a)** Discuss arithmetic, logic and shift microoperations in brief. **07**

(b) Write brief note on "Instruction codes" **07**

OR

Q.5 **(a)** What is scratchpad memory? Explain the working of a processor unit employing a scratchpad memory with diagram. **07**

(b) Answer the following questions: **07**

1. What are the advantages & disadvantages of hard-wired control and microprogram control?
2. Write brief note on "Typical characteristics of IC logic families'.

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