Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–III • EXAMINATION – SUMMER 2013

Subject Code: X 30902 **Date: 13-05-2013**

Subject Name: Analog and Digital Electronics

Time: 02.30 pm - 05.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw and Explain the use of op-amp as a Schmitt trigger.	**07**
	(b)	Sketch the circuit of Op-amp as Integrator and explain with necessary waveforms.	**07**
Q.2	**(a)**	Explain ideal Inverting & Non-inverting amplifier.	**07**
	(b)	Draw Block Diagram of an Op-amp. Explain Function of each block.	**07**
		OR	
	(b)	List and discuss characteristics of an ideal Op-amp.	**07**
Q.3	**(a)**	Sketch the diagram of 555 timers as a Monostable Multivibrator. Explain its working and derive equation for frequency of output waveform.	**07**
	(b)	Classify IC Voltage regulators. Explain Basic three terminal IC regulators with the help of Block diagram.	**07**
		OR	
Q.3	**(a)**	Prove that NOR and NAND gates are universal.	**07**
	(b)	State & Explain De'Morgan's 1st & 2nd Law.	**07**
Q.4	**(a)**	What do you mean by a K map? List its advantages and disadvantages.	**07**
	(b)	Describe J K flip flop. How J-K flip-flop differ from S-R flip-flop?	**07**
		OR	
Q.4	**(a)**	Explain operations of S-R flip flop with the help of logic symbol, circuit diagram and truth table.	**07**
	(b)	Classify Shift registers. Explain Serial In Parallel Out and Parallel In Parallel Out shift register.	**07**
Q.5	**(a)**	What is Decoder? Explain 3 to 8 decoder circuit using truth table and logic diagram.	**07**
	(b)	Explain Weighted Resistor type DAC converter	**07**
		OR	
Q.5	**(a)**	List the various logic families available and explain in brief the specifications of Digital IC'S.	**07**
	(b)	Derive Full Adder with necessary truth table & K-Map. Also express it with AOI logic diagram.	**07**

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