Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–VI • EXAMINATION – SUMMER • 2014

Subject Code: X 61102 **Date: 30-05-2014**

Subject Name: VLSI Technology and Design

Time: 10:30 am - 01:00 pm **Total Marks: 70**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Derive the expression of threshold voltage of nMOS transistor.	**07**
	(b)	Write a short note on short channel effects	**07**
Q.2	**(a)**	Explain the following scaling methods of MOSFETs (i) constant-field scaling (ii)constant-voltage scaling	**07**
	(b)	Write a short note on MOSFET capacitances	**07**
		OR	
	(b)	Explain the models networks used for calculation of interconnect delay.	**07**
Q.3	**(a)**	Explain working of CMOS inverter.	**07**
	(b)	Derive the expression of Switching power dissipation of CMOS inverter.	**07**
		OR	
Q.3	**(a)**	Define the following terms of an inverter with diagrams: (i) ζ_{PHL} (ii) ζ_{PLH} (iii) Rise time (iv) Fall time	**07**
	(b)	Draw the CMOS circuit for the following Boolean function: Z = (A(D + E) + BC)) ‘	**07**
Q.4	**(a)**	Write a short note on CMOS transmission gate.	**07**
	(b)	What is voltage bootstrapping in dynamic logic circuits? Explain.	**07**
		OR	
Q.4	**(a)**	Explain the dynamic CMOS logic (Precharge – evaluate) logic.	**07**
	(b)	Give examples of the following types of faults in a typical VLSI circuit: (i)Physical (ii)Electrical (iii)Logical	**07**
Q.5	**(a)**	Explain the basic fabrication steps in manufacturing a typical CMOS transistor.	**07**
	(b)	Explain the VLSI design flow in structural, behavioral and geometric domain.	**07**
		OR	
Q.5	**(a)**	Write a short note on FPGA.	**07**
	(b)	Draw CMOS SR latch circuit based on NOR2 gates and explain its function.	**07**

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