Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER– II EXAMINATION – SUMMER 2015

Subject Code: X21102 **Date:03/06/2015**

Subject Name: Digital logic design

Time: 10.30am-01.00pm **Total Marks: 70**

Instructions:

1. **Attempt any five questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Do as directed: (i) $(1010.011)_2 = (\quad)_{10}$ (ii) $(362.35)_8 = (\quad)_{10}$ (iii) $(25.625)_{10} = (\quad)_2$ (iv) $(101.101)_2 = (\quad)_{10}$ (v) $(42AD)_{16} = (\quad)_{10}$ (vi) $(92.85)_{10} = (\quad)_{16}$ (vii) $(3642)_8 = (\quad)_{10}$	**07**
	(b)	Explain basic theorems of Boolean algebra with example.	**07**
Q.2	**(a)**	Explain Arithmetic addition and Arithmetic subtraction with some suitable example.	**07**
	(b)	Which gates are called as the universal gates? Explain with logic diagram, characteristic table.	**07**
Q.3	**(a)**	Write short note on four bit Universal Shift Register.	**07**
	(b)	Explain briefly : SOP & POS , minterm & maxterm , canonical form	**07**
Q.4	**(a)**	Explain in detail ROM and PLA	**07**
	(b)	What is parity? Explain parity generation and checking in detail.	**07**
Q.5	**(a)**	Describe JK and T flip-flops with logic diagram, characteristic table and characteristic equation.	**07**
	(b)	Explain briefly RS and D flip-flops.	**07**
Q.6	**(a)**	Explain BCD Ripple counter and draw its logic diagram and timing diagram.	**07**
	(b)	Write a short note on Encoder.	**07**
Q.7	**(a)**	Explain in detail introduction of Control Logic Design.	**07**
	(b)	Draw and explain logic diagram of arithmetic logic unit (ALU).	**07**

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