Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–VI • EXAMINATION – SUMMER • 2015

Subject code: X61102 Date: 12/05/2015

Subject Name: VLSI Technology and Design

Time:10:30 am - 01:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Discuss VLSI design flow in behavioural,structural and geometrical layout domain. **07**

(b) Discuss packaging concerns for VLSI chips.Give examples of common IC packages. **07**

Q.2 **(a)** Explain the following operating regions of MOS system under external bias:Accumulation,Depletion,Inversion **07**

(b) Consider a MOS system with the following parameters: **07**

tox = 200 A^o ,ϕ_{GC} = -0.85 V,N_A =2 x 10^{15} cm^{-3} ,Qox= q x 2 x 10^{11} C/cm^2

(i)Determine the threshold voltage V_{T0} under zero bias at room temperature (T = 300 K). Note that $\varepsilon_{ox} = 3.97\ \varepsilon_0$ and $\varepsilon_{si} = 11.7\ \varepsilon_0$.

(ii)Determine the type (p-type or n-type) and amount of channel implant (N_I/cm^2) required to change the threshold voltage to 0.8 V.

OR

(b) Consider a diffusion area which has the dimensions 10 μm x 5 μm, and the abrupt junction depth is 0.5 μm. Its n-type impurity doping level is N_D = 1 x 10^{20} cm^{-3} and the surrounding p-type substrate doping level is N_A = 1 x 10^{16} cm^{-3}. Determine the capacitance when the diffusion area is biased at 5 V and the substrate is biased at 0 V. In this problem, assume that there is no channel-stop implant. **07**

Q.3 **(a)** Discuss small and narrow channel effects in a MOS transistor. **07**

(b) Design a resistive-load inverter with R= 1 kΩ, such that V_{OL}= 0.6 V. The enhancement-type nMOS driver transistor has the following parameters: **07**

V_{DD} = 5.0 V , V_{T0} = 1.0 V , γ = 0.2 $V^{1/2}$,λ = 0, μn Cox = 22.0 μA/V^2

(i)Determine the required aspect ratio, W / L.

(ii)Determine V_{IL} and V_{IH}

(iii)Determine noise margins NM_L and NM_H.

OR

Q.3 **(a)** Define the critical voltages V_{IL},V_{IH}, V_{OL} and V_{OH} and noise margins for an inverter. **07**

(b) Consider a CMOS inverter circuit with the following parameters: **07**

V_{DD} = 3.3 V , $V_{To.}$,n = 0.6 V, $V_{To.}$,p = —0.7 V,kn = 200 μA/V^2 , kp = 80 μA/V^2

Calculate the noise margins of the circuit.

Q.4 **(a)** Prove that the average power dissipation in a CMOS inverter is directly proportional to the operating frequency. **07**

(b) Write a short note on CMOS transmission gates. **07**

OR

Q.4 **(a)** Draw the circuit of CMOS SR latch based on NOR2 gates and explain. **07**

(b) Explain the basic Principles of Pass transistor circuits. **07**

Q.5 **(a)** What are the high performance dynamic CMOS circuits?Explain any one. **07**

	(b)	Write a short note on Electrostatic Discharge protection circuits in VLSI chip.	**07**

OR

Q.5	**(a)**	Explain constant field and constant voltage scaling.	**07**
	(b)	Write a short note on FPGA and CPLD.	**07**

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