Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC-Semester –VI (May-2012) Examination

Subject code: X61102

Subject Name: VLSI Technology and Design

Date:09 /05/2012

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Draw and explain Y chart of VLSI design flow. **07**

(b) Define following terms **07**

(1) Moore's Law (2) Threshold voltage (3) Set up time
(4) Controllability (5) Punch through
(6) FPGA (7) Observability

Q.2 **(a)** Explain n-well CMOS process with necessary sketches. **07**

(b) What is scaling? Why it is required? Explain full scaling. **07**

OR

(b) For an n-channel MOS transistor $\mu_n = 700\ cm^2 / Vs$, **07**
$Cox = 8 .10^{-8}\ F/cm^2$ W= 20µm, L= 2 µm , $V_{TO} = 0.78V$.
To calculate drain current at
(a) $V_{GS} = 2V$ and $V_{DS} = 1V$
(b) $V_{GS} = 3V$ and $V_{DS} = 4V$

Q.3 **(a)** Explain MOS capacitance. **07**

(b) Explain MOS system under external bias with necessary diagram **07**

OR

Q.3 **(a)** Derive equation of dynamic power dissipation of CMOS inverter. **07**

(b) Consider a resistive load inverter circuit with VDD =5V, $k'_n = 20\mu A/v^2$, V_{TO} = 0.8V, R_L = 200Kohm and W/L = 2. Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) on the VTC and find the noise margins of circuit. **07**

Q.4 **(a)** A CMOS inverter has $V_{TO,n} = 0.8$ V, $V_{TO,p} = -0.8$ V , and $k_n = k_p$. Obtain V_{IL}, V_{IH}, V_{OH},V_{OL} , NM_H and NM_L for $V_{DD} = 5v$ **07**

(b) Draw and explain VTC of depletion load inverter. **07**

OR

Q.4 **(a)** Explain Voltage bootstrapping with necessary derivation and diagram. State disadvantages of it. **07**

(b) Explain CMOS Transmission gate with necessary figure and equation. **07**

Q.5 **(a)** Draw CMOS implementation for following Boolean equation. **07**

$$P(S + T) + QR)'$$

Assume that (W/L)n = 10 for all nMOS and (W/L)p =15 for all pMOS. Find (W/L) ratio for nMOS and pMOS.

(b) Draw and explain Master- slave D flip-flop using CMOS implementation. **07**

OR

Q.5 **(a)** Explain Latch up in brief and gives its prevention **07**

(b) Explain BIST. **07**

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