Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC– SEMESTER II– • EXAMINATION –WINTER- 2016

Subject Code: X21102 **Date:03/01/2017**

Subject Name: Digital Logic Design

Time:02:30 PM to 5:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Do a directed 1) $(25.25)_{10} = (\ )_2$ 2) $(123.45)_8 = (\ )_{10}$ 3) $(2112)_{10} = (\ )_{16}$ 4) $(1011110.101)_2 = (\ )_{10}$ 5) $(AB.CD)_{16} = (\ )_8$ 6) 11011 x 1010 = $(\ )_2$ 7) What is difference between binary code and gray code?	**07**
	(b)	Define the following terms: Noise margin, Propagation delay, Fan-out, Literal, Power dissipation, Canonical form, Minterms.	**07**
Q.2	**(a)**	State and prove De Morgan's Theorems with the help of truth tables.	**07**
	(b)	Prove universality of NAND & NOR gate.	**07**
		OR	
	(b)	Explain basic theorems of Boolean algebra with example.	**07**
Q.3	**(a)**	Simplify the function using K-map. $Y = \sum m(0,1,5,9,13,14,15) + d(3,4,7,10,11)$ & draw logic diagram.	**07**
	(b)	What is race around condition? Explain the Master-Slave J-K flip-flop.	**07**
		OR	
Q.3	**(a)**	Determine the prime implicants of the function using tabulation method $F(W, X, Y, Z) = \Sigma(1, 4, 6, 7, 8, 9, 10, 11, 15)$	**07**
	(b)	Draw & explain full adder circuit with truth table and logic diagram.	**07**
Q.4	**(a)**	Explain operation of 8:1 multiplexer with block diagram & truth table. Also implement it using gates.	**07**
	(b)	Design a combinational circuit that converts 4 bit Binary code to 4 bit Gray code.	**07**
		OR	
Q.4	**(a)**	With logic diagram & truth table explain the working of 3 to 8 line decoder.	**07**
	(b)	Design a combinational circuit whose input is 3 bit binary number and output is square of that number.	**07**
Q.5	**(a)**	Explain 4-bit bidirectional shift register with parallel load in detail.	**07**
	(b)	Design Mod 10 Counter using J-K Flip flop.	**07**
		OR	
Q.5	**(a)**	Give & explain classification of Logic families.	**07**
	(b)	Design BCD ripple counter using Toggle flip flop.	**07**

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