Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER– VI • EXAMINATION – WINTER 2016

Subject Code: X 61102 **Date:26/11/2016**

Subject Name: VLSI Technology and Design

Time: 10.30 AM - 01.00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	State Moore's Law and Explain full semicustom and full custom design.	**07**
	(b)	Explain the Local Oxidation of Silicon (LOCOS) technique for MOSFET fabrication and discuss the bird's beak problem.	**07**
Q.2	**(a)**	Explain depletion, Inversion and channel creation for MOSFET with necessary diagram.	**07**
	(b)	What is scaling and why it is required in MOSFET technology. Explain voltage scaling in detail.	**07**
		OR	
	(b)	Explain the short-channel effect in detail.	**07**
Q.3	**(a)**	Draw and explain VTC of resistive load inverter.	**07**
	(b)	Define the critical voltages V_{IL},V_{IH}, V_{OL} and V_{OH} and Noise margins for an inverter.	**07**
		OR	
Q.3	**(a)**	Define TPLH and TPHL. Derive equation of TPHL for CMOS inverter.	**07**
	(b)	Explain the basic Principles of Pass transistor circuits and discuss it with examples.	**07**
Q.4	**(a)**	Draw the CMOS circuit for the following Boolean function: $Z = (A(D + E) + BC))$ '	**07**
	(b)	Explain Voltage bootstrapping with necessary derivation and diagram.	**07**
		OR	
Q.4	**(a)**	Explain the Precharge and evaluate mechanism for dynamic CMOS logic.	**07**
	(b)	Draw and explain Master- slave D flip-flop using CMOS implementation.	**07**
Q.5	**(a)**	Explain built in self test (BIST).	**07**
	(b)	Explain CMOS Latch up problems. Suggest remedies for it.	**07**
		OR	
Q.5	**(a)**	Explain the on chip clock distribution techniques.	**07**
	(b)	Draw and explain architecture of FPGA and CPLD.	**07**

****