Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC– SEMESTER VII– • EXAMINATION – SUMMER - 2016

Subject Code: X71105 **Date:18/11/ 2016**

Subject Name: Embedded System (Department Elective-I)

Time:10:30 AM to 1:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Briefly explain load and store architecture of ARM.	**07**
	(b)	Define embedded system. Briefly discus embedded system design constraints.	**07**
Q.2	**(a)**	Draw and explain the structure of the ARM cross-development toolkit.	**07**
	(b)	Explain ASR and LDMIA ARM instruction by giving examples.	**07**
		OR	
	(b)	Explain ARMs visible registers with figure. Briefly explain CPSR.	**07**
Q.3	**(a)**	Give classification of embedded systems. Explain each in detail.	**07**
	(b)	Write a short note on 3-stage pipeline ARM organization.	**07**
		OR	
Q.3	**(a)**	Draw and discuss the basic block diagram of architectural model of ARM controller.	**07**
	(b)	Discuss thumb data processing instructions in detail.	**07**
Q.4	**(a)**	Explain the difference between Real Time Clock and Watch Dog Timer related to embedded systems.	**07**
	(b)	Write short note on OS security issues.	**07**
		OR	
Q.4	**(a)**	Explain synchronous, iso-synchronous and asynchronous serial communication modes with suitable example.	**07**
	(b)	Discuss the difference between Process, Thread and Task with respect to real time operating system (RTOs).	**07**
Q.5	**(a)**	Write short note on: USB Bus.	**07**
	(b)	What are the situations, which lead to priority inversion and deadlock problems? How does it resolved?	**07**
		OR	
Q.5	**(a)**	Write short note on: HTTP Bus.	**07**
	(b)	What are the situations, which lead to priority inversion and deadlock?	**07**

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