GUJARAT TECHNOLOGICAL UNIVERSITY
PDDC - SEMESTER – II • EXAMINATION – WINTER 2012

Subject code: X 21102   **Date: 24/01/2013**
Subject Name: Digital Logic Design
Time: 10.30 am - 01.00 pm   **Total Marks: 70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	1.	Represent $(8620)_{10}$ (i) in BCD, (ii) in excess-3 code, and (iii) as a binary number.	**03**
		2.	$(3322.2)_4 = ($ $)_{10}= ($ $)_{16}$	**02**
		3.	$(B6)_{16}+(40)_8=($ $)_7$	**02**
	(b)	1.	Define and explain the duality principal. Find the complement of the function $F = x'$ $(yz+y'z')$ using duality principal.	**03**
		2.	Multiply the $(296)_{12}$ and $(57)_{12}$ in the given base without converting to decimal.	**02**
		3.	Perform subtraction $(56.25)_{10}-(17.12)_{10}$ using 10's complement.	**02**
Q.2	**(a)**		Demonstrate by means of truth tables the validity of the De Morgan's theorems for three variables. Find the complement of the Boolean function $F (A, B, C, D) = (BC'+A'D) (AB'+CD')$ and reduce them to a minimum number of literals.	**07**
	(b)		Answer the followings:	**07**
		1.	Simplify the Boolean function: $F(A,B,C,D,E) = \Sigma m (0,1,4,5,16,17,21,25,29)$ using Karnaugh map.	
		2.	Implement Boolean function $F= (A +B') (CD+E)$ using only NAND gates.	

OR

	(b)		Simplify the Boolean function $F(w,x,y,z)=\Sigma m(1,4,6,7,8,9,10,11,15)$ using tabulation method.	**07**
Q.3	**(a)**		Design a combinational circuit whose input is a four-bit number and whose output is the 2's complement of the input number.	**07**
	(b)		Write brief technical note on:	**07**
		1.	Read-Only Memory (ROM)	
		2.	Basic Flip-Flop circuit	

OR

Q.3	**(a)**		Explain BCD adder in detail.	**07**
	(b)		Answer the following questions:	**07**
		1.	Design a BCD-to-decimal decoder.	
		2.	Implement Boolean function $F(A,B,C)=\Sigma m(1,3,5,6)$ using 4:1 multiplexer.	

Q.4 **(a)** Draw the clocked Master-Slave J-K flip-flop configuration and explain how it removes race-around condition in J-K flip-flops.   **07**

(b) Design a counter with the binary sequence: 0, 4, 2, 1, 6 and repeat. Use JK flip-flops.   **07**

OR

Q.4 **(a)** Write detail note on Shift registers.   **07**

(b) Explain BCD ripple counter with logic diagram and timing diagram.   **07**

Q.5 **(a)** Describe in brief: **07**
    1.   4-stage switch-tail ring counter
    2.   4-bit ALU (Arithmetic Logic Unit)

(b) List out all methods of control organization and explain any one method in detail.   **07**

OR

Q.5 **(a)** Describe Instruction codes in brief. Also compare macrooperations and microoperations.   **07**

(b) Explain block diagram of a processor unit with its operation.   **07**

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