Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER – III • EXAMINATION – WINTER 2012

Subject code: X 30902 **Date: 28/12/2012**

Subject Name: Analog and Digital Electronics

Time: 10.30 am - 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is op-amp? Discuss four basic building blocks of an op-amp and list the characteristics of an ideal op-amp.	**07**
	(b)	Define and Explain the following terms. (1) Input offset voltage (2) Output voltage swing (3) CMRR (4) Gain Bandwidth Product	**07**
Q.2	**(a)**	Why op-amps are not used in open loop configuration for linear application? What do you understand by negative feedback?	**07**
	(b)	Draw circuit of a closed loop non-inverting amplifier and derive formula for voltage gain with feedback.	**07**
		OR	
	(b)	An *IC741* op-amp is connected in voltage shunt feedback configuration. $R_1 = 470\ \Omega$ and $R_F = 4.7\ k\ \Omega$. Calculate the values of A_F, R_{iF}, R_{oF}, f_F and V_{ooT}. Op-amp specifications are given as, $A=200000$, $R_i=2\ M\ \Omega$, $R_o=75\ \Omega$, $f_o=5\ Hz$. Supply voltage = $\pm 15\ V$ and output voltage swing = $\pm 13\ V$	**07**
Q.3	**(a)**	Draw high frequency model of an op-amp and express *open-loop voltage gain* as a function of frequency. What is corner frequency?	**07**
	(b)	Discuss op-amp application as a First-order high-pass Butterworth filter.	**07**
		OR	
Q.3	**(a)**	Explain : Summing Amplifier both inverting and non-inverting configuration. What modifications are required to obtain weighted sum of signals?	**07**
	(b)	Explain : *IC 555* as a Monostable Multivibrator.	**07**
Q.4	**(a)**	Show how *AND* and *OR* gate can be fabricated using (1) only *NAND* gates (2) only *NOR* gates.	**07**
	(b)	Discuss : De Morgan's theorems.	**07**
		OR	
Q.4	**(a)**	(1) Use 12 bit 2's complement method to subtract 79.625 from 27.125. (2) Convert $(756.603)_8$ to hexadecimal.	**07**
Q.4	**(b)**	With the help of neat circuit diagram, explain the working of a *Two Input TTL NAND Gate.*	**07**
Q.5	**(a)**	Reduce the expression $\sum$ m(0,2,3,4,5,6) using K-map and implement it using AOI logic as well as NAND logic.	**07**
	(b)	Draw logic diagram of a Full Adder using AOI logic, NAND logic and NOR logic.	**07**
		OR	
Q.5	**(a)**	Define the following terms as applied to flip-flops. (1) Set-up time (2) Hold time (3) Propagation delay (4) maximum clock frequency	**07**
	(b)	What is a register? What is a shift register? What are the types of shift registers? Briefly discuss the applications of shift registers.	**07**

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