Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–II • EXAMINATION – WINTER 2013

Subject Code: X21102 Date: 23-12-2013

Subject Name: Digital Logic Design

Time: 02.30 pm - 05.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Do as directed: **07**

1. $(11011.101)_2$ = ($)_{10}$
2. $(378.93)_{10}$=($)_8$
3. $(5637.534)_8$ = ($)_{16}$
4. Determine the value of base b if $(35)_{10} = (50)_b$
5. $(1032)_4$=($)_5$
6. Find dual of: x+0=x
7. Find the 10's complement of $(4069)_{10}$.

(b) Answer the following questions: **07**

1 Multiply $(367)_8$ and $(715)_8$ in the given base without converting to decimal.

2 What is the difference between canonical form and standard form? Reduce the Boolean expressions F(A,B,C,D)=[(CD)'+A]'+A+CD+AB to three literals.

Q.2 **(a)** Answer the following questions: **07**

1 Perform subtraction $(4AB.68)_{16}$-$(507D.56)_{16}$ using the 16's complement method.

2 Simplify the Boolean function F(A,B,C,D) = AB'C+B+BD'+ABD'+A'C to a minimum number of literals by manipulation of Boolean algebra.

(b) Show that NAND gate is universal gate. Simplify the Boolean function F(A,B,C,D) = AC'+ABC+AB'C+A'CD'+A'B'D' using Karnaugh map and implement it with no more than three NAND gates. Assume that both the normal and complement inputs are available. **07**

OR

(b) What are called don't-care conditions? Design a combinational circuit that multiplies by 5 an input decimal digit represented in BCD. The output is also in BCD. Show that the output can be obtained from the input lines without using any logic gates. **07**

Q.3 **(a)** Find the prime-implicants of the function F(w,x,y,z)=Σm(0,1,6,7,8,9,13,14,15). **07**

(b) Answer the following questions: **07**

1 Construct a 5 × 32 decoder with four 3 × 8 decoder and a 2 × 4 decoder. Use block diagram construction only.

2 Explain programmable logic array.

OR

Q.3 **(a)** Design a BCD-to-excess-3 code converter. **07**

(b) Design a 4-bit BCD adder using two 4-bit binary adders. How many don't-care inputs are there in a BCD adder? **07**

Q.4 **(a)** Design a counter using JK flip-flops that has a repeated sequence of six states: 0, 1, 2, 4, 5, 6. Determine the effect of unused states. **07**

	(b)	Answer the following questions: 1 Write a technical note on: Clocked RS Flip-Flop 2 Draw a logic diagram of 4-bit register with parallel load	**07**
		OR	
Q.4	**(a)**	What is race around condition in flip flops? Explain operation of the D-type positive-edge triggered flip-flop.	**07**
	(b)	Implement and explain a 4-bit binary ripple up-counter using flip-flops that trigger on the negative edge.	**07**
Q.5	**(a)**	Explain Johnson counter and generation of timing signals in detail.	**07**
	(b)	Explain in brief: 1. Fixed-point binary data and floating-point data. 2. Arithmetic shifts	**07**
		OR	
Q.5	**(a)**	Explain the design of Arithmetic Logic Unit	**07**
	(b)	Explain one flip-flop per state method of control organization with diagram.	**07**

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