Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–VI • EXAMINATION – WINTER 2013

Subject Code: X61102 **Date: 06-12-2013**

Subject Name: VLSI Technology and Design

Time: 02.30 pm - 05.00 pm **Total Marks: 70**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Give difference between semicustom and full custom design.	**07**
	(b)	Draw and explain Y chart of VLSI design flow. Also draw simplified flow of VLSI design flow.	**07**
Q.2	**(a)**	Derive current - voltage equation for NMOS.	**07**
	(b)	Explain n-well CMOS Process with necessary sketches.	**07**
		OR	
	(b)	Explain following terms in short. 1) Controllability. 2) Moore's law. 3) Punch through 4) Noise Margin 5) CPLD 6) Set up time. 7) Hold time.	**07**
Q.3	**(a)**	Draw and explain architecture of FPGA.	**07**
	(b)	Draw CMOS and depletion NMOS load implementation for following Boolean equation **1)** $Z = \overline{ADE + BC}$ **2)** $Z = \overline{A + DE + BC}$	**07**
		OR	
Q.3	**(a)**	Explain voltage scaling. Explain effect of voltage scaling on drain current, power dissipation and power density.	**07**
	(b)	Draw and explain VTC of CMOS inverter.	**07**
Q.4	**(a)**	Draw and explain VTC of resistive load inverter.	**07**
	(b)	Derive equation of T_{PLH} and T_{PHL} for CMOS inverter.	**07**
		OR	
Q.4	**(a)**	Draw and explain working of CMOS transmission gate. Also explain characteristics of CMOS transmission gate.	**07**
Q.4	**(b)**	Discuss basic principal of pass transistor circuits.	**07**
Q.5	**(a)**	Draw and explain on chip clock generation and distribution.	**07**
	(b)	What is Latch-up problem in CMOS inverter? Write its prevention.	**07**
		OR	
Q.5	**(a)**	Explain CMOS dynamic circuits techniques.	**07**
	(b)	Draw and explain JK latch using CMOS implementation	**07**

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