Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–II • EXAMINATION – WINTER • 2014

Subject Code: X21102 Date: 30-12-2014

Subject Name: Digital Logic Design

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following questions: **07**

1. $(73.375)_{10}$ = ( )$_2$
2. $(46155)_{10}$=( )$_{16}$
3. $(1E9.FC)_{16}$ = ( )$_8$
4. $(100101.10001)_2$ = ( )$_{10}$
5. Obtain 10's complement of $(09900)_{10}$.
6. What is difference between BCD code and binary code?
7. Add $(18D)_{16}$ and $(75)_{16}$ without converting to decimal.

(b) Answer the following questions: **07**

1. State duality principle.
2. Simplify the Boolean function F=x+x'y to a minimum number of literals.
3. Simplify the Boolean function F=a'bc+ac+a'c to a minimum number of literals.
4. Prove that: (AB+C+D)(C'+D)=ABC'+D
5. Find the complement of the function F=A'B'C+AB'C'
6. Show that the dual of the excusive-OR is equal to its complement.
7. Differentiate between combinational logic circuit and sequential logic circuit.

Q.2 **(a)** Answer the following questions: (3+2+2) Marks **07**

1. Perform the subtraction $(100)_2$-$(110000)_2$ using 1's complement.
2. Demonstrate by means of truth table the validity of the distributive law of + over ·.
3. Implement Boolean function F = (A +B) (C+D)E using only NOR gates. Assume that both the normal and complement inputs are available.

(b) Simplify the Boolean function F= w'(x'y + x'y'+ xyz) +x'z' (y+w) using don't-care conditions d=w'x (y'z + yz') + wyz in (i) sum of products and (ii) product of sums using Karnaugh map. **07**

OR

(b) Design a combinational circuit with four input lines that represent a decimal digit in BCD and four output lines that generate the 9's complement of the input digit. **07**

Q.3 **(a)** Simplify the Boolean function $F(x_1,x_2,x_3,x_4)=\Sigma m(0,5,7,8,9,10,11,14,15)$ using tabulation method. **07**

(b) Write brief note on "Full adder" and explain carry propagation in binary parallel adder. **07**

OR

Q.3 **(a)** Design a counter with the binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use T flip-flops. Determine the effect of unused states. **07**

(b) Write brief note on (i) 3-to-8 line decoder (ii) Types of ROMs **07**

Q.4 **(a)** Draw a logic diagram of master-slave flip-flop and explain timing relationships in a master-slave flip-flop. **07**

(b) Answer the following questions: **07**

1 Obtain an 8×1 multiplexer with a dual 4-line to 1-line multiplexers having separate enable inputs but common selection lines. Use block diagram construction.

2 Explain 3-stage switch-tail ring counter.

OR

Q.4 **(a)** Explain concept of shift registers and discuss 4-bit bidirectional shift register with parallel load. **07**

(b) Explain BCD ripple counter with timing diagram. Also draw a block diagram of a 3-decade decimal BCD counter. **07**

Q.5 **(a)** Explain control logic with sequence register and decoder with diagram in detail. **07**

(b) Answer the following questions: (3+2+2) Marks **07**

1 What is scratchpad memory?

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2 Write instruction-code formats.

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3 What is the difference between hard-wired control and microprogram control?

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OR

Q.5 **(a)** Write brief note on "Status register" and explain block diagram of an 8-bit ALU with a 4-bit status register. **07**

(b) Classify microoperations most often encountered in digital systems and explain any one in detail. **07**

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