Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–III • EXAMINATION – WINTER • 2014

Subject Code: X30902 **Date: 29-12-2014**

Subject Name: Analog and Digital Electronics

Time: 10:30 am - 01:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What are the feedback configurations? Draw an Op-amp Inverting amplifier circuit and obtain the frequency response curve for it. Derive an expression for it.	**07**
	(b)	Sketch the circuit of Op-amp as Differentiator and explain with necessary waveforms.	**07**
Q.2	**(a)**	Draw the circuit for dual input balanced output differential amplifier using constant current bias circuit. Why current mirror circuit preferred to constant current bias for differential amplifier.	**07**
	(b)	Define and explain the following Op-amp parameters and state the Ideal Op Amp conditions: (1) Input offset current (2) Input bias current. (3) Slew rate. (4) PSRR	**07**
		OR	
	(b)	Discuss universality of NOR gate, also Derive all gates with the help of NOR gate.	**07**
Q.3	**(a)**	What do you mean by input offset voltage? Draw and explain offset voltage compensating network.	**07**
	(b)	Explain the full adder with help of circuit diagram using NAND gate write the truth table.	**07**
		OR	
Q.3	**(a)**	Explain De'Morgans theorems giving necessary logic expressions and diagrams.	**07**
	(b)	Explain the working of Master-Slave J-K flip-flop.	**07**
Q.4	**(a)**	Sketch the diagram of 555 timers as an astable Multivibrator. Explain its working and derive equation for frequency of output waveform.	**07**
	(b)	What do you mean by a K map? List it's advantages and disadvantages.	**07**
		OR	
Q.4	**(a)**	With sketch realize the expression X = AB + CD using (i) NAND gates only and (ii) NOR gates only	**07**
	(b)	Compare the CMOS and TTL logic.	**07**
Q.5	**(a)**	Draw functional block diagram of IC 555 & discuss function of each pin.	**07**
	(b)	Discuss multiplexers & demultiplexers with suitable diagram.	**07**
		OR	
Q.5	**(a)**	Explain the working of PLL using appropriate block diagram and explain any one application of the same.	**07**
	(b)	With the help of neat circuit diagram explain the working of: (i) A two input TTL NAND gate (ii) A two input CMOS NOR gate.	**07**

****