Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

PDDC - SEMESTER–VI • EXAMINATION – WINTER • 2014

Subject Code: X61102 Date: 02-12-2014

Subject Name: VLSI Technology and Design

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** In the context of the design of a VLSI chip discuss the following criteria: **07**
(i)Testability (ii)Yield and manufacturability
(iii)Reliability (iv)Technology updateability

(b) Explain the Local Oxidation of Silicon (LOCOS) technique for fabricating MOSFET. **07**

Q.2 **(a)** Obtain the expression of the drain current of an n-channel MOSFET using Gradual channel Approximation model. **07**

(b) Calculate the threshold voltage V_{TO} at V_{SB} = 0,for a polysilicon gate n-channel transistor with the following parameters:Substrate doping $N_A = 10^{16}$ cm^{-3} ,polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3} , gate oxide thickness t_{ox}= 500 A^0 , and oxide –interface charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}. **07**

OR

(b) Measured voltage and current data for a MOSFET are given below.Determine the type of the device, and calculate the parameters k_n , V_{TO} and γ. Assume ϕ_F = -0.3 V. **07**

V_{GS}(V)	V_{DS}(V)	V_{SB} (V)	I_D (μA)
3	3	0	97
4	4	0	235
5	5	0	433
3	3	3	59
4	4	3	173
5	5	3	347

Q.3 **(a)** Derive the expressions of noise margins NM_L and NM_H for a resistive load inverter. **07**

(b) Calculate the equivalent W/L for the two nMOS with W_1/L , W_2/L connected in series.Neglect the body effect. **07**

OR

Q.3 **(a)** Define the critical voltages V_{IL},V_{IH}, V_{OL} and V_{OH} and noise margins for an inverter. **07**

(b) Consider a resistive load inverter circuit with V_{DD} = 5 V , k'_n = 20 μA/V^2 , V_{TO} = 0.8V, R_L = 200 kΩ , and W/L = 2. Calculate the critical voltages(V_{OL}, V_{OH}, V_{IL} , V_{IH}) on the VTC and find the noise margins of the circuit. **07**

Q.4 **(a)** A store has one express register and three regular ones.It is the store policy that the express register is open only when two or more of the other registers are busy.Assume that the Boolean variables A,B and C reflect the status of each of the regular registers(1 busy, 0 idle). Design the logic circuit , with A,B and C as inputs and F as output , to automatically notify the manager (by setting F=1) to open the express register.Present two solutions , the first using only NAND gates , the second using only NOR gates. **07**

(b) Derive the expression of threshold level V_{TH} of 2-input NOR2 CMOS inverter. **07**

OR

Q.4 **(a)** Discuss synchronous dynamic logic circuits techniques. **07**

(b) Write a short note on domino CMOS. **07**

Q.5 **(a)** Discuss the onchip clock generation and distribution for a VLSI chip. **07**

(b) Write a short note on out put circuits and L(di/dt) noise. **07**

OR

Q.5 **(a)** What are the various concerns of the packaging technology of a VLSI chip? Give examples of the various packages. **07**

(b) Derive the expression of frequency of oscillation of a CMOS ring oscillator. **07**

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