Gujarat Technological University

Organizes

A Two Day's workshop on VLSI Technology
At

L.D. College of Engineering

(25th and 26th February, 2012)

In association with

A Two Day's workshop on VLSI Technology

About CoreEL Technologies

CoreEL Technologies is a technology company with businesses spread across design services & product development, distribution and training. Head Quartered in Bangalore, India, CoreEL is a leading provider of VLSI & Embedded System design services and Intellectual Property. Since its inception in 1999, CoreEL Technologies a privately held corporation has always strived to deliver quality solutions & support in all the business areas that it serves.

Our Services offerings include Distribution of Silicon solutions, EDA tools, COTS products, Engineering Services (Turn Key Systems Design, Turn Key FPGA Design and High Speed PCB Design), Education and Manufacturing. These services are offered to our broad customer base comprising Defense and Aerospace, Telecommunication and Networking, Homeland Security, Broadcast Video and Education segments.

CoreEL University Program

CoreEL University Program as the name suggests, has a mandate to reach out to the larger talent pool in the Indian universities. It comprises of a dedicated team of professionals who possess rich design and application engineering experience in VLSI, Embedded and related areas. With its core team at Bangalore and regional offices in key cities across the country, the University solutions group draws its strength from its established design services teams and from Sandeepani-India's No. 1 VLSI design school. The group's association with world leaders such as Xilinx, Mentor Graphics, Opal RT, WindRiver, (VxWorks), Kontron, IBM Rational SEED Program etc., makes it a formidable force in providing solutions in the University space. CoreEL University Program offers distribution of world class VLSI Development Platforms & EDA tools and technical support to academia community which includes

- VLSI Lab infrastructure setup assistance as per the course curriculum of institutions
- EDA Tools installation and enabling the tools utilization through customized training offerings
- Domain specific workshop modules to address the requirements of research enthusiasts
- Technical support services for academia community in their R & D activities

Agenda

The Two day workshop is aimed at providing in depth coverage of ASIC Full custom IC Design flow and FPGA design flow. The program offers ample amount of opportunities to explore the concepts with exhaustive hands-on sessions with Mentor Graphics EDA Tool flow and Xilinx FPGA flow.

How to Register

- All Engineering faculties from EC department can participate in this program. Send Registration form by e-mail mentioning "workshop on VLSI Technology" subject on the secvc@gtu.ac.in on or before 13th February, 2012.

Highlights

- Digital IC design flow using Mentor EDA tool flow
- Concepts of Functional Verification and basic test bench architecture
- Synthesis, simulation mismatches - a study using Modelsim, Leonardo Spectrum and precision RTL
- Xilinx FPGA architecture and Design flow
- Hardware debugging using Xilinx Chipscope ILA and VIO
- Overview of Xilinx Embedded Design flow and DSP System Generator
- Focus on backend design flow with relevant details on physical design & verification
- Overview of parasitic extraction and back annotation using Calibre

PRE-REQUISITE FOR PROGRAM

The participants are familiar with the following pre-requisites:

- Basic ASIC & FPGA design flow

- Exposure to concepts of HDL

- Concepts of CMOS Analog and Digital design

<u>Schedule</u>

Day1:

Session I: 8:30 am to 9:00 am

- Registration

Morning Session:

Session I: 9:00 am to 10:45am

- An overview of ASIC & FPGA flow – a perspective of industry and academia
- Introduction to Mentor Graphics EDA flow

Tea Break: 10:45am to 11:00am

Session II: 11:00am to 1:00pm

- Lab 1: Hands-on session on concepts of design entry, functional simulation and ASIC and FPGA synthesis
- Concepts of Full custom & semicustom IC Design flow

Lunch Break: 1pm to 2pm

Afternoon Session:

Session III: 2:00pm to 3:30pm

- Lab 2: Hands-on session on schematic entry and schematic and layout simulations
- Lab 3: Concepts of physical verification – Hands on session on LVS checks

Tea Break: 03:45pm to 4:00pm

Session IV: 4:00pm to 5:30pm

- Lab 4: Physical Verification using Calibre & Post Layout Simulation using ELDO. Concepts of parasitic extraction and back annotation
- Overview of Netlist to GDS flow

Q/A Session: 5:30pm to 6:00pm

Day 2:

Morning Session:

Session V: 9:00 am to 10:45am

- FPGA architecture & Design flow: Xilinx perspective
- Lab 1: Xilinx FPGA Design flow using Xilinx ISE and its exploring its features – Project Navigator, Xpower Analyzer and Plan Ahead

Tea Break: 10:45am to 11:00am

Session VI: 11:00am to 1:00pm

- Hardware debugging using Xilinx Chipscope PRO (ILA and VIO)
- Lab 2: Hardware Debugging using Chipscope PRO

Lunch Break: 1pm to 2pm

Afternoon Session:

Session VII: 2:00pm to 3:45pm

- Overview of Xilinx Embedded Design flow and features of EDK and SDK
- Lab 3: Demonstration of Embedded System Modeling using EDK and overview of SDK

Tea Break: 03:45pm to 4:00pm

Session IV: 4:00pm to 5:30pm

- DSP Design flow using Xilinx System Generator with MATLAB/Simulink
- Lab 4: Demonstration of Integration of Xilinx System Generator with MATLAB/Simulink and performing hardware co-simulation

Q/A Session: 5:30pm to 6:00pm

Technical Resource persons:

Damodara M S, Product Manager & Ramesh Dasara, Field Application Engineer from CoreEL Technologies India Pvt. Ltd.