e-Prayog
Virtual Labs (Electronics), IIT Bombay
Wadhwani Electronics Lab

An initiative of Ministry of Human Resource Development (MHRD) under the National Mission on Education through ICT

Two Days workshop on Modern Digital Design

On

3rd & 4th December 2012

Organized by

Gujarat Technological University, Ahmedabad

in association with,
e-Prayog Virtual Labs (Electronics),
IIT Bombay,
Mumbai – 400076

Venue of the Workshop:

L J Institute of Engineering & Technology
L J Campus
Between Kataria Motor and Sanand-Sarkhej Circle,
S. G. Highway, Ahmedabad-382210,
Gujarat, India.

Course Co-ordinator (GTU)
Dr. Kiran Parmar
Professor, EC Dept
LDCE, Ahmedabad
09825489790

Course Co-ordinator (IIT Bombay)
Ms. Madhumita Date
Project Manager, e-Prayog,
Wadhwani Electronics Lab,
IIT Bombay
098199688511

Who Should Attend?

Faculty members of only GTU affiliated colleges, who have taught and will be teaching "VLSI Technology and Design" for the Spring Semester 2013.

Course Fee:

No course fee for the participants. TA/DA will not be reimbursed.

Note

Each interested participating institute will be provided with **FIVE Krypton** boards (worth Rs. 7000/ each) **FREE OF COST** to conduct the lab in their institute. Free remote CPLD lab environment will in installed at selected institutes.

All the GTU affiliated colleges' Directors/Principals are requested to kindly nominate at least one faculty from your college, so that your institute can benefit from this workshop.

Teaching Faculty

e-Prayog team from Wadhwani Electronics Lab, Department of Electrical Engineering, IIT Bombay.

Registration

For the Registration kindly visit the below link:

https://docs.google.com/a/gtu.edu.in/spreadsheet/viewform?formkey=dHRCd0FUZWNhclRTMWVWSWpFaGg1N3c6MQ

Please submit your filled form on or before 24 /11/2012.

For any query please contact:

079 – 26300699/40200618

CPLD lab developed by e-Prayog

With rapid development of programmable logic devices, it has become mandatory to teach the concepts of reconfigurable hardware at the undergraduate level. Though some universities have already improved their teaching facilities in this area, a first course in digital logic design has been difficult mainly due to challenges in scaling up of the laboratory facilities at UG level. In many colleges the students' experience is limited to emulation, and they do not get a hands-on experience with these devices.
The e-Prayog team provides a low-cost solution to teach concepts of digital design using a CPLD board with minimal requirements on the student's part.

The main objectives of the CPLD Lab developed by e-Prayog are:

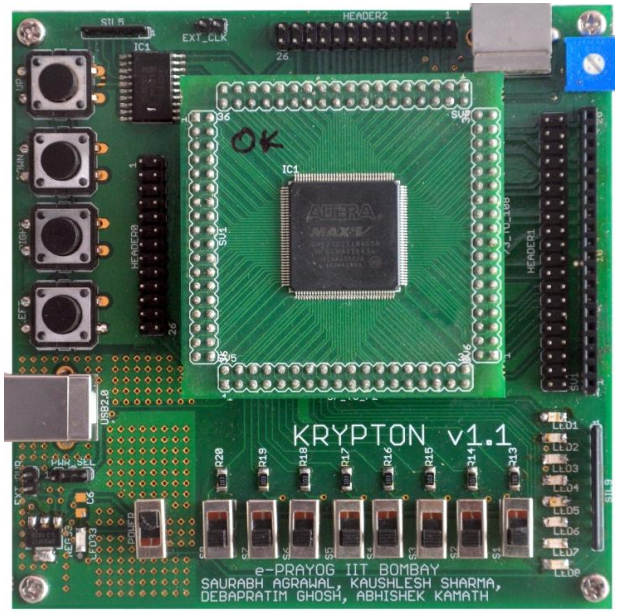
- To give students hands-on experience with the process of reconfigurable logic design, implementation, and verification of logic systems using modern designing tools for digital logic design using an affordable CPLD board designed by e-Prayog.
- To make the student confident in using state-of-the- art technology.
- To provide remote access to the CPLD board developed by e-Prayog.

About the workshop

The objective of this workshop is to give hands-on experience to the participants on implementation and verification of logic design using the "krypton" (CPLD) board designed and developed by e-Prayog. The workshop is specially designed to suit the GTU curriculum and is expected to cover more than 75% laboratory requirement of the course "VLSI Technology and Design" taught in VI Semester to ECE/Electronics branches.

Krypton is also suitable for mini projects which are an important part of the syllabus.

Krypton



Workshop Schedule

Day-1 (03.12.2012)	
8.30 am	Registration and Inauguration
9:00 am	Introduction to e-Prayog, IIT Bombay
10.30 am	Introduction to Reconfigurable Design Introduction to Quartus- II
2.00 pm	**Lab session:** • Implementation of Serial Adder • Implementation of Binary Counter
3:45 pm	**Lab session:** • 4:1 MUX and 3:8 Decoder • Implementation of BCD Counter • 8 bit Multiplier • Demo of remote CPLD Lab
Day-2 (04.12.2012)	
9.00 am	**Lab Session:** (Interfacing Experiments) • Tone Generator • Interfacing 16X2 Character LCD • Interfacing PS2 & VGA Monitor • Demo of GLCD
2.00 pm	**Lab Session:** (Design a small system) • Interfacing ADC • Interfacing DAC • Interfacing temperature sensor and displaying the temperature on LCD