Report of

Workshop on HPC & Parallel Programming

organized by

Gujarat Technological University

in collaborate with

C-DAC & Intel Software

At

Gujarat Technological University

On

20th June-2015

Under the visionary leadership of Honorable Vice Chancellor Dr. Akshai Aggarwal, Gujarat Technological University has successfully organized one day workshop on HPC & Parallel processing in collaboration with C-DAC & Intel Software on 20th June-2015. To conduct this workshop, Mr. Chitranjan Singh & Ms. Shweta Das from C-DAC HPCS Group and Mr. Om Sachan from Intel Software, were present to share their knowledge and experience.

Objective of the workshop

Supercomputing is seen as a powerful tool for a nation to compete with other nations. Government of India has launched the National Supercomputing Mission envisaged to enable India to leapfrog to the league of world class computing power nations.

The Mission enables to empower national academic and R&D institutions spread over the country by installing a vast supercomputing grid comprising of more than 70 high-performance computing facilities. The Mission also includes development of highly professional High Performance Computing (HPC) aware human resource for meeting challenges of development of these applications.

To support such kind of massive HPC infrastructure to be created during the mission in the country, the manpower should also have to be geared up accordingly. To empower our scientific community to be HPC ready, C-DAC is conducting a series of parallel programming workshops nationwide.

Workshop Abstract

The one-day workshop aims to create HPC and parallel programming knowhow amongst academicians, scientists, researchers and engineers and how it can benefit them. It will provide a detailed outline of HPC overview which includes building blocks, applications, and parallel programming models, software development tools, emerging technologies and trends as well as growth opportunities in HPC.

The main concepts and technologies talked about will include computer architectures, clusters, computing with many-core architectures (GPGPUs and Xeon Phi), SIMD, Vectorization, MPI, Open MP and development tools such as compilers, profilers, advisors.

The workshop was initiated by welcoming all experts and given an introduction of the experts to all participants by Mr. Naresh Gardas (C-DAC). Mr. Naresh Jadeja, deputy director of GTU welcomes all experts and participants.

First Session:

Ms. Shweta Das initiates workshop with brief explanation about High Performance Computing (HPC) .High Performance Computing (HPC) is the game changer for scientific and engineering research resulting in innovation and better approach, leading to human advancement in terms of well-being, social advantage and wealth creation. It also enables us to address the opportunities and challenges that lie ahead.

HPC in general, refers to the practice of aggregating computing power in a way that delivers much higher performance than one could get out of a typical desktop computer in order to solve large problems in science, engineering, or business in much shorter time. Numerous scientific and engineering breakthroughs have been accomplished with the help of HPC.

HPC plays a vital role in addressing several grand challenge problems like climate modeling, oceanography, seismic analysis, life sciences, astrophysics, materials modeling, structural mechanics etc., which cannot be executed by ordinary computers in a stipulated time envelope. Supercomputing facilities have enabled countries in their science and technology capabilities in areas such as designing vehicles, aero planes, massive structures like high rise buildings and bridges, infrastructure, discovery of new life saving drugs, discovery and extraction of new energy sources including oil, natural gas etc.

Most importantly HPC which is relying on the parallel processing Paradigm's has moved into Industry domains and has been used in Pringle chips design, Good Year all Weather Tyres, P&G Diapers and Golf Balls Design to many other day to day product design efforts bringing revolutionary innovations and speed to the market. These applications of HPC have generated several new avenues of employment for fresher's and experienced to migrate to challenging roles of Parallel programming with higher income levels.

Second Session:

Second session was started by Mr. Chitranjan Singh with below mention building blocks of HPC.

Requirement of HPC:

- High speed because of Grand Challenge problems
- Novel applications which are not possible otherwise
- Strategic and Technology advancement
- Scalability : More processors more power
- Human Advancement: Economy

About Parallel Architecture:

- Single Instruction Single Data (SISD) Sequential Machines
- Multiple Instructions Single Data (MISD)
- Single Instruction Multiple Data (SIMD)
  Array of processors with single control unit
- Multiple Instructions Multiple Data (MIMD)
  Several Processors with several Instructions and Data Stream.
- Tightly Coupled MIMD & Loosely Coupled MIMD
- Latency and Bandwidth
- Single Processor Parallelism (use more pipelines, use more cores in same die, use of advanced extensions)
- Multi-Processor Parallelism - Shared Memory (use of multiple processors to speed up program run-time, by dividing up the entire computation among the processors)

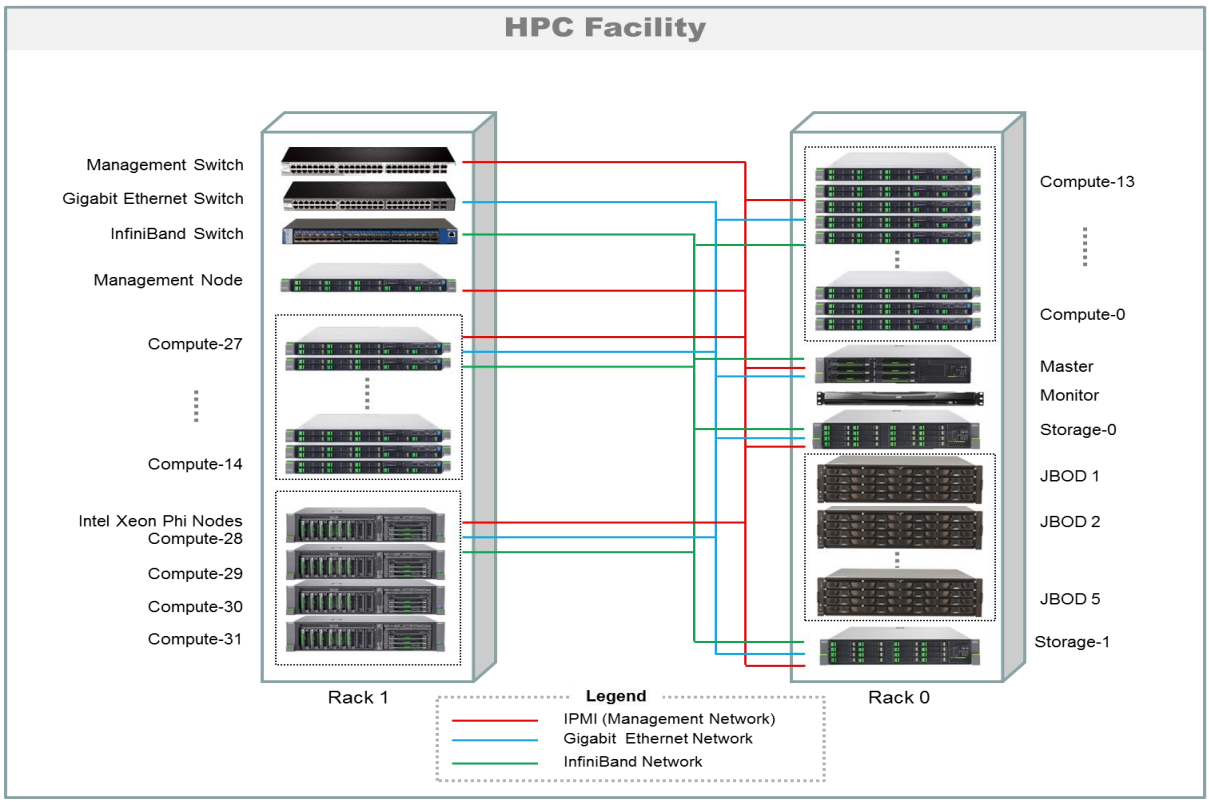
Components of a cluster computer and HPC:

- Head Node / Master
- Compute Node /Slave
- Cluster Software
- Cluster Interconnect
- Cluster Storage

Brief discussed about PARAM SHAVAK super computer:

- Supercomputer in a Box system in a table top model
- Powered with 2 multicore CPUs each with at least 10 cores along with either one or two numbers of accelerator cards
- 2 Tera-flops and above computing power with 5 terabytes and above storage
- Easy to deploy solution with minimum datacentre infrastructure.
- Pre-loaded with parallel programming development tools and libraries
- Preinstalled indigenous scheduling and resource management tools

- Tutorials, learning material, videos and user manuals, etc.
- Built-in selected Scientific & Engineering Applications across several HPC application domains.



Third Session:

Third Session was taken by Mr. Om Sachan from Intel about following:

About Intel Parallel Studio XE 2015:

Faster Code

- Explicit vector programming speeds more code
- Optimizations for Intel® Xeon Phi™ coprocessor, Sky lake and Broad well microarchitecture
- MPI library now supports latest MPI-3 standard
- Faster processing of small matrixes
- Parallel direct sparse solvers for clusters

Code Faster

- Comprehensive compiler optimization reports
- Analyze Windows* or Linux* profile data on a Mac*

Latest standards support

- MPI-3, OpenMP 4, Full C++11 and Fortran 2003

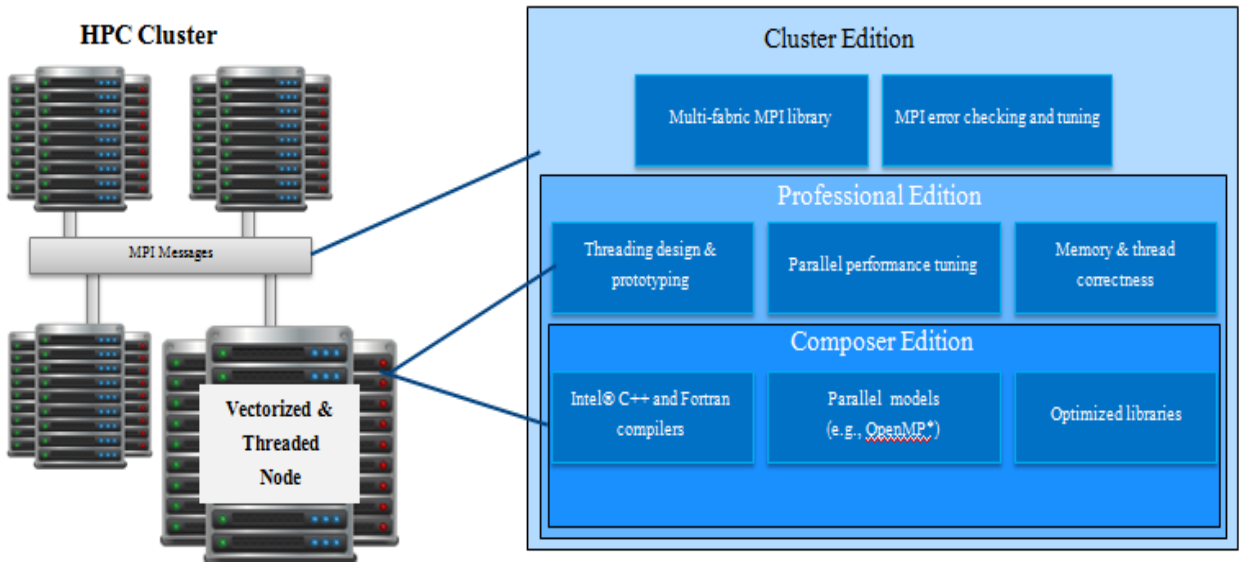
Vector and parallel programming improvements

- Explicit vectorization achieves predictable vectorization
- Similar to what OpenMP* does for parallelization
- Maps threaded execution to SIMD hardware
- Memory alias and alignment analysis improvements
- Expanded alignment and restrict attributes

Hardware Support

- Sky lake support
- Knights Landing (KNL) support
- Compute on Intel Graphics

Standards: Full C++ 2011, Full Fortran 2003 support, Fortran 2008 BLOCK support, OpenMP* 4.0



Intel® C++ and Fortran Compilers 15.0:

- Common for both
  - New OpenMP 4.0 vectorization simplifies taking advantage of SIMD instructions for great performance on Intel® Xeon® and Xeon Phi™ processors and coprocessors

- Improved compiler optimization reports help quickly identify optimization opportunities. For Windows-based developers, Visual Studio* 2010, 2012 and 2013 integration is included.
- Linux*, OS X*, Windows*, Android*
- Available now in a variety of configurations to suit different development needs. C++ Info Fortran Info

- Intel® C++ Compiler
  - Intel Cilk™ Plus keywords for parallelism simplify implementation of task and data parallelism
  - Complete C++11 support
- Intel® Fortran Compiler
  - Support for the latest Fortran standards
  - Rogue Wave* IMSL* Fortran Numerical Libraries: Performance add-on for Intel® Fortran Windows suites

List of Top-10 Super Computers in World:

Rank	Site	System	Cores	Rmax (TFlop/s)	Rpeak (TFlop/s)	Power (kW)
1	National Super Computer Center in Guangzhou, China	Tianhe-2 (MilkyWay-2)	3120000	33862.7	54902.4	17808
2	DOE/SC/Oak Ridge National Laboratory, US	Titan- Cray XK7	560640	17590	27112.5	8209
3	DOE/NNSA/LLNL United States	Sequoia- BlueGene/Q	1572864	17173.2	20132.7	7890
4	RIKEN Advanced Institute for Computational Science (AICS) Japan	K computer	705024	10510	11280.4	12659.9
5	DOE/SC/Argonne National Laboratory, US	Mira- BlueGene/Q	786432	8586.6	10066.3	3945
6	Swiss National Supercomputing Centre (CSCS), Switzerland	Piz Daint- Cray XC30	115984	6271	7788.9	2325
7	Texas Advanced Computing Center/Univ. of Texas United States	Stampede	462462	5168.1	8520.1	4510
8	Forschungszentrum Juelich (FZJ) Germany	JUQUEEN- BlueGene/Q	458752	5008.9	5872	2301
9	DOE/NNSA/LLNL United States	Vulcan- BlueGene/Q	393216	4293.3	5033.2	1972
10	Government United States	Cray CS-Storm	72800	3577	6131.8	1498.9

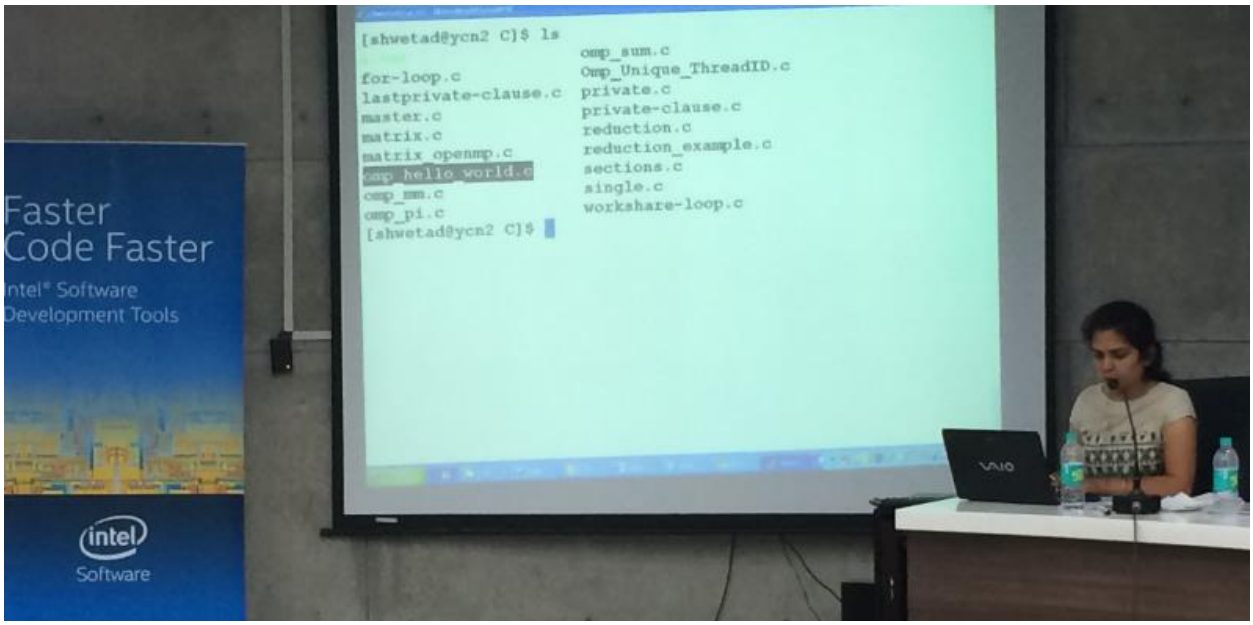
List of Top-10 Super Computers in India:

Rank	Site	R_{max} TFLOPS	Top 500 Rank
1	Indian Institute of Tropical Meteorology, Pune (iDataPlex System)	719.2	71
2	Center for Development of Advanced Computing (C-DAC), Pune	386.71	131
3	Indian Institute of Technology, Kanpur	295.25	149
4	CSIR Fourth Paradigm Institute (CSIR-4PI), Bangalore	334.38	155
5	National Centre For Medium Range Weather Forecasting, Noida	318.4	163
6	Vikram Sarabhai Space Centre (VSSC), Indian Space Research Organization (ISRO, Trivandrum	188.7	346
7	Tata Consultancy Services Pvt. Ltd., Pune	132.8	389
8	Indian Institute of Technology, Madras	75.5	Not in top 500
9	S.N. Bose National Centre for Basic Sciences, Kolkata	60.00	Not in top 500
10	Indian Institute of Tropical Meteorology, Pune (IBM Cluster)	45.84	Not in top 500

The entire session was successfully delivered by all the three experts. At last technical quiz was conducted by the experts and then prize of Book (High Performance Parallelism Pearls by Jim Jeffers and James Jeffers) was given to the winners. Workshop ended by presented the vote of thanks to experts, participants and students of the GTU PG School for their valuable support.

WORKSHOP PHOTO GALLERY

Keynote by Mr. Naresh Jadeja (Deputy Director, GTU)



Session delivered by Ms. Shweta Das

Session delivered by Mr. Chitranjan Singh

Participants attending sessions

Participants attending sessions