C-DAC &Gujarat Technological University
M.E. Electronics & Communication Engineering
(VLSI & Embedded Systems Design)
Gandhinagar

Semester – II

2725204: Designing with Modeling & FPGA's (Elective II & III)

UNIT I – Review of transistor operation, Single stage amplifiers, Differential amplifier
MOS I/V characteristics. Transistor second order effects. Small signal analysis. Small signal model.Gain of common-source stage amplifier using small signal analysis. Common-source stage with resistive load, diode-connected load, current-source load, triode load, source degeneration. Source follower stage. Common-gate stage. Cascode stages.Single-ended and differential operation. Basic differential pair.Common-mode response. Differential pair with MOS loads. Gilbert Cell.

UNIT II - Current Mirrors, Response of Amplifiers, Noise characteristics
Basic and cascode current mirrors. Using active current mirrors as loads. The Miller theorem. Frequency response of source follower, common-gate amplifier, cascode stage, differential pair.Noise characteristics. Noise types: thermal noise, flicker noise. Representation of noise in circuits. Properties of feedback circuits. Feedback Configurations. Effect of loading in feedback

UNIT III - Operational amplifiers
Operational amplifier's performance parameters. One-Stage Op Amps. Two-Stage Op Amp. Op Amps Gain Boosting. Op Amps Common-Mode Feedback. Op Amps Input Range Limitation: unity-gain buffer, extension of input CM range, variation of equivalent transconductance with the input CM level. Op Amps Slew Rate. Noise in Op Amps and Power Supply Rejection.Stability and Frequency compensation.

UNIT IV - Bandgap References, Switched-capacitor circuits,Nonlinearity
Supply-independent biasing. Temperature- independent references: negative-TC voltage, positive-TC voltage, bandgap reference. PTAT current generation. Speed and noise issues. Continuous-time feedback amplifier using resistors, capacitors, switched-capacitor amplifier in sampling mode, amplification mode, transfer of capacitor's charges. Sampling switches. Switched-capacitor amplifiers. Switched-capacitor integrator. Nonlinearity. Mismatch. Ring oscillators. LC oscillators. Voltage-controlled oscillators. Mathematical models of VCOs.

UNIT V- Phase-locked loops, Data converters, charge-coupled devices (CCD)
Simple PLL.Charge-pump PLLs.Non ideal effects in PLLs: PFD/CP non idealities, jitter in PLLs.Delay-locked loops.PLL applications. Analog versus discrete time signals. Sample and hold characteristics.ADC and DAC
specifications.DAC architectures.ADC architectures. Sampling and aliasing, Quantization noise & Data Converter SNR. CCD imaging and architecture.

UNIT VI- Modeling with FPGA

Logic modeling – Memory modeling, Bus Function Modeling (BFMs), System modeling- Proof of Concept, Timed and untimed functions and their interactions, TLM, IP core models and simulation, Synthesizable modeling, Case studies – Parameterized Flip-Flop, DDR/QDR Memory

Labs:

Tools used during laboratory exercises are Custom Designer, WaveView and HSpice, Modelsim.

References:

1. R.J. Baker, H.W. Li, D.E. Boyce. CMOS. Circuit design, Layout, and Simulation (2nd Edition), 2005. 1038p.
2. P. Horowitz, W. Hill, Electronic Circuit Design: Art and Practice, 2001. 192p.
3. B. Razavi, Design of Analog CMOS Integrated Circuits, 2000. 684p.
4. R.J. Baker, CMOS Mixed-Signal Circuit Design, 2002. 502p
   B. Razavi. Principles of Data Conversion System Design. 1994. 272P