C-DAC &Gujarat Technological University
M.E. Electronics & Communication Engineering
(VLSI & Embedded Systems Design)
Gandhinagar

Semester – II

2725203: Digital VLSI Design – II Backend (Elective II & III)

UNIT I – Recap of Front-end flow and Logic Synthesis.
Recap Units II and IV of Course Digital VLSI Design I – Front-end.

UNIT II – Physical Design Setup and Floorplanning
VLSI Design Cycle, Methodology of Physical Design, Simplified Cycle of Physical IC Design, Partitioning, Floorplanning, Placement, Routing, Compaction, Verification. Logical libraries, Physical Libraries, Timing Constraints, Database format, Logical data setup, Physical data setup, Technology Files, Interconnect delay models, tcl scripting for automation. Hierarchical Design Planning Flow, Pad Creation and Order Assignments, Core Area, Initializing the Floorplan, Timing Driven Placement, Placement with Hierarchical Gravity, Analyze placement and Color Modules, Post-initialization Macro placement controls, Large Macro Handling, Power Network Synthesis (PNS), Power Network Analysis (PNA).

UNIT III – Placement
Placement Methodology, Fast Iteration with Coarse Placement, Understanding the Congestion Calculation, Textual Congestion Report, Analyzing the Congestion Map, Global Route (GR) for Congestion Map, Strategies for Fixing Congestion Problems, Congestion-Driven Placement Options, Adjusting Cell Density, Timing and Power Optimization for Best QoR, Congestion-Driven Placement, Incremental Congestion Refinement, Refinement Flow, Incremental mode, Area Recovery, Timing Analysis.

UNIT IV – Clock Tree Synthesis
Design Status, Start of CTS Phase, Clock Tree Synthesis, CTS Goals, Define Clock Root Attributes, Stop, Float and Exclude Pins, Generated and Gated Clocks , User-defined or Explicit Stop Pins, Defining an Explicit Float Pin, Preserving Pre-Existing Clock Trees, Impact of Preexisting Clock Cells, Logical Design Rule Constraints, Non-Default Clock Routing, Specifying Non-Default Rules, Non-default Rule Options, Effects of Clock Tree Synthesis, Incremental Placement / Optimization, Analysis using the CTS GUI , Clock Tree Optimization, Inter-Clock Delay Balancing, Post Route CTO.

UNIT V – Routing and Post Tapeout flow
Design Status, Start of Routing Phase, Grid-Based Routing System, Routing over Macros, Pre-Route Checks, Routing Operations, Core Routing Strategy, Fixing DRC Violations, Crosstalk-Induced Noise, Crosstalk-Induced Delay, Crosstalk Prevention, Crosstalk Correction, Wire Sizing.

Labs:
Tools used during laboratory works: Design Compiler and IC Compiler.

References:

1. J.P. Uyenmura. Introduction to VLSI Circuits and Systems, J.Wiley & Sons, 2002.
2. J.M. Rabaey, A. Chandrakasan, B. Nikolic. Digital Integrated Circuits – A Design Perspective, Prentice Hall, 2003.
3. J.P. Uyenmura. Modern VLSI Design - System-on-Chip Design, Prentice-Hall, 2002.