



**C-DAC & Gujarat Technological University**  
**M.E. Electronics & Communication Engineering**  
**(VLSI & Embedded Systems Design)**  
**Gandhinagar**

**Semester – II**

**2725205: System on Chip Architecture(Elective II & III)**

**UNIT – 0 SoC methodology**

Abstract system modeling – Introduction to Transaction Level Modeling(TLM), SystemC, High Level Synthesis (HLS), specification, Requirement analysis related to power, performance and cost – Algorithms, architecture, implementation constraints; control and data path analysis, partitioning; interfacing requirements; Integration and Verification, Regression testing

**Part – I System on FPGA**

**UNIT – I**

Embedded hard and soft processor cores in FPGAs from Altera, Xilinx and others; Interfacing processor core with user FPGA logic, IP cores and interface to processor bus, Booting methods, configuration and parametric customization, debugging, design environment, base system builder, hardware simulation flow, supported OS and porting effort, Processor bus bridging to support reusable IPs/peripherals, Case study- AXI4 bus specification; Memory organization – Internal and external memory controller design, cross-compilers for HLL programming, provision for custom instructions, Auxiliary processing units

**UNIT – II Case Study**

Xilinx Zynq family overview, system development methodology, use of the ARM processor features like Neon, MMU, floating point unit, exception handling; Developing AXI4 based peripheral using FPGA fabric

**Part – II System on Chip**

**UNIT – I**

Requirement analysis, Classification of SoC, Comparative study of different SoC platforms from TI, freescale, cavium, Tiler, intel, nvidia, Qualcomm, Cypress, netronome, ezchip and more etc...- Key features, accelerator engines, application domains like graphics, DSP, image processing, audio-video encoding-decoding, security, encryption-decryption, Power efficiency, performance criteria;

**UNIT – II Case Study**

Cypress PSoC family; Overview, system development methodology, Analog mixed signal design flow; Case studies – Analog sensing, DSP, memory access, networking, PWM; hardware-software co-design

**Labs:**

Tools used during laboratory works: Xilinx zynq EDK, cypress psoc development environment, keil software

**References:**

1. Zynq data sheets [www.xilinx.com](http://www.xilinx.com)
2. PSoC documentation [www.cypress.com/psoc](http://www.cypress.com/psoc)