GUJARAT TECHNOLOGICAL UNIVERSITY

M.E. - Electronics & Communication Engineering
(VLSI &Embedded Systems Design)
Semester: I

Subject Name**: Digital VLSI Design I - Frontend**
Subject Code**: 715202**

Objective:

The study of IC design basics, levels, strategies, options, methods, styles, challenges, economics and trends especially front-end. In the process of the laboratory work it is necessary to study the main front-end IC design tools and to implement in the basic digital electronic circuits design.

Lecture:

UNIT I - Introduction - Levels of IC design – Digital circuit fundamentals

Concept of IC. IC structure, components, applications. History and evolution of the IC industry. Moore's Law. Design economics - Nonrecurring engineering costs (NRE) & Recurring costs, Yield & Technology scaling.

System level Design. Top down design. Bottom up design. Back end design. Design abstraction levels. Behavior Level. Register-Transfer Level (RTL). Logic Level. Circuit Level. Component level. Examples of Domains and its Abstraction Levels.

CMOS logic gates, Combinational circuits, Sequential circuits, FSM

UNIT II - Design Flow

Design flow: Frontend – Marketing Requirements, Design specification, Verification plan, RTL description, Functional verification, Synthesis. Backend – Partitioning, Floor planning, Placement, CTS, Routing & layout generation, layout verification, Tapeout. Foundry - Fabrication

Introduction to Testing – Need for testing, manufacturing test, design for test, chip-level test, system-level test, test generation & fault models

Introduction to System on chip (Soc) design - Soft cores, Firm cores, Hard cores. Study of AMBA AXI4 protocol.

UNIT III - IC Design techniques & options, CAD design, Design challenges

Structured design techniques: hierarchy, regularity, modularity, locality.

Design options: Programmable logic Design, sea of gates and gate array design, standard cell design, full-custom design. Study of FPGA tools.

Using of CAD tools: Behavioral synthesis tool, RTL synthesis tool , logic optimization tool, structural to layout synthesis tool, layout synthesis tool, design capture tools, design verification tools, circuit extractor, design rule checker (DRC), electrical rule checker (ERC), layout vs. schematic.

Design challenges –
Microscopic issues: ultra-high speeds, power dissipation, supply rail drop, importance of inter connect, noise, crosstalk, reliability, manufacturability, clock distribution.
Macroscopic issues: time to market, design complexity, high levels of abstractions, reuse, IP, portability, tool interoperability.
Sub-nm technologies: technology scaling, switching power reduction, leakage power control, process variations, die to die frequency variation, temperature variation.

UNIT IV- Digital Design and Synthesis

Verilog HDL. Concepts of Design planning, RTL design for Sequential & combinational circuits, State machines design & encoding. Simulation , waveform generation, coverage reports.

Synthesis concepts, Technology libraries, Constraints, Netlist generation & optimization.

UNIT V – Design verification using System Verilog & VMM

System Verilog – Verification guidelines, Data types, Interfaces, Assertions, Randomization, Coverage

Concepts of verification, verification plan, test cases & testbench generation

VMM – Layered test bench architecture: Signal, Command, Functional, Scenario & Test layers

Lab:

Tools used during laboratory works: VCS & Design Compiler

- Study and implementation using VCS and Design Compiler

Course Project:

A project of suitable complexity, comprising of RTL design, Testbench formation and coverage must be completed by the student.

Course Material:

The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

Reference Books:

1. Synopsys recommended course material and lectures.
2. N. Weste, K. Eshragyan. Principles of CMOS VLSI Design. Adisson Wesley, 1993
3. J.F. Wakerly. Digital Design - Principles & Practices, Prentice Hall, 2001
4. Digital logic design by Morris Mano
5. Verilog HDL: A guide to digital design & synthesis, 2e by Samir Palnitkar
6. System Verilog for verification, 2e by Chris Spear – Springer
7. IEEE Std 1364™-2005 - Verilog LRM
8. System Verilog LRM

9. System Verilog Golden reference guide