GUJARAT TECHNOLOGICAL UNIVERSITY
M.E. Semester: 4
Specialization: Signal Processing and VLSI Technology
Branch: Electronics and Communication Engineering

Subject: VLSI Test Principles and Architectures

SR NO.	COURSE CONTENTS
1.	**Introduction:** Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.
2.	**Design and Testability:** Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability.
3.	**Logic and Fault Simulation:** Introduction, Simulation Models, Logic Simulation, Fault Simulation,
4.	**Test Generation:** Introduction, Random Test Generation, Theoretical Background: Boolean Difference, designing a Stuck-At ATPG for Combinational Circuits, Designing a Sequential ATPG, Untestable Fault Identification, Designing a Simulation-Based ATPG, Advanced Simulation-Based ATPG, Hybrid Deterministic and Simulation-Based ATPG, ATPG for Non-Stuck-At Faults, Other Topics in test Generation.
5.	**Logic Built-In Self-Test:** Introduction, BIST Design Rule, Test Pattern Generation, Output Response Analysis, Logic BIST Architectures, Fault Coverage Enhancement, BIST Timing /Control, Design Practice.

Reference Books:

1. VLSI Test Principles and Architectures, Wang Wu Wen, Morgan Kaufmann Publishers.
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.
3. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing and Testable Design", IEEE Press, 1990.
4. T.Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000.
5. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification- Methodology and Techniques", Kluwer Academic Publishers, 2001.